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The CLAS12 Silicon Vertex Tracker

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ABSTRACT

For the 12 GeV upgrade of Jefferson Laboratory, a Silicon Vertex Tracker (SVT) has been designed for the CLAS12 spectrometer using single-sided microstrip sensors fabricated by Hamamatsu Photonics. The sensors have a graded angle design to minimize dead areas and a readout pitch of 156 μm, with intermediate strips. Each double-sided SVT module hosts three daisy-chained sensors on each side with a full strip length of 33 cm. There are 512 channels per module, read out by four Fermilab Silicon Strip Readout (FSSR2) chips, featuring data-driven architecture, mounted on a rigid–flex hybrid board. The modules are assembled in a barrel configuration using a unique cantilevered geometry to minimize the amount of material in the tracking volume. This paper is focused on the design, qualification of the performance, and experience in operating and commissioning the tracker during the first year of the data taking.

1. Physics requirements and technical specifications

Essential parts of the Jefferson Laboratory (JLab) Hall B CLAS12 [1] physics program, such as the measurement of parton distribution functions, require tracking of low-momentum particles with a few percent momentum resolution and about one degree angle resolution at large angles [2]. Stable operation of the tracker at instantaneous luminosities up to 10^{35} cm^{-2} s^{-1} is required over a period of roughly ten years. These requirements are achieved by the central tracker, installed inside the CLAS12 5 T superconducting solenoid magnet [3], providing a highly uniform field in the tracking volume and acting as a Møller electron shield.

Silicon detector technology provides an excellent match to the central tracking system in the CLAS12 configuration, where limited space is available and high-luminosity operation is needed for accurate measurements of exclusive processes at high momentum transfer. The silicon energy band gap (1.12 eV at room temperature) is large enough to have a low leakage current due to electron–hole pair generation, while it is small enough to allow production of a large number of charge carriers per unit energy loss of the ionizing particles. The large energy loss per traversed length of the ionizing particle (3.8 MeV/cm for a minimum-ionizing particle) due to the high material density (2.33 g/cm^3) leads to production of measurable signals in thin detectors. Because of the high mobility of electrons and holes, silicon detectors can be used in high-rate environments, with charge collection times on the order of ns. These characteristics are the main decisive factors leading to large-area applications of silicon sensors for tracking devices. The expected integrated luminosity per year in CLAS12 is 500 fb^{-1}. The radiation dose for the CLAS12 Silicon Vertex Tracker (SVT) sensors (carbon target) is 2.5 Mrads over a period of 15 years.

The SVT provides tracking capabilities in the CLAS12 Central Detector by measuring recoil baryons, large angle pions, kaons, and protons, with tracking efficiency ≥90%, transverse momentum resolution $\delta p_T/p_T \leq 5\%$, and angular resolution for polar angles $\delta\theta \leq$ 10–20 mrad (within 35°–125°) and azimuthal angles $\delta\phi \leq 5$ mrad (within ≥90% of 2π). The CLAS12 Central Detector consists of the SVT as the inner detector, surrounded by the Barrel Micromegas Tracker (BMT) [4], the Central Time-Of-Flight system (CTOF) [5], and the Central Neutron Detector (CND) [6]. The required momentum resolution is provided by the SVT, while the BMT improves the polar angle resolution due to the strips crossing at 90°. Note that together the SVT and BMT systems form the CLAS12 Central Vertex Tracker (CVT).

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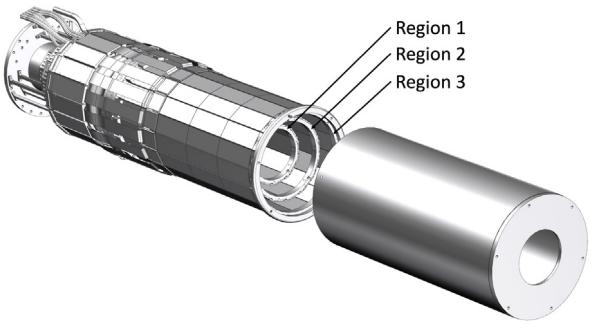

Fig. 1. Layout of the SVT barrel and the Faraday cage. Copper supports are bolted directly to the upstream cold plate. The beam enters along the SVT axis from the left.

Tracks are matched up with hits in the CTOF system for β vs. p measurements (particle identification). The SVT allows for reconstruction of detached vertices, e.g. $K^0_s \to \pi^+\pi^-$, $\Lambda \to \pi^- p$, $\Xi \to \Lambda\pi$, for an efficient experimental program in strangeness physics.

To satisfy the physics requirements on track momentum resolution, the SVT must have low mass inside the acceptance region. The SVT module position tolerances should be within 20, 500, and 100 μm across the module, along the module, and along the beam, respectively.

2. Design

2.1. Barrel layout and support structure

The SVT is comprised of 21,504 channels of wire-bonded triplets of p-on-n, AC-coupled, single-sided silicon microstrip sensors in six layers. The SVT barrel is formed by three concentric polygonal regions of double-sided SVT modules, positioned at radii of 65, 93, and 120 mm (see Fig. 1). The innermost Region 1 layer contains 10 modules, encircled by Region 2 with 14 modules, and Region 3 with 18 modules. The SVT is enclosed by a Faraday cage with an inner radius of 57 mm (with 6 mm clearance to the inner shell of the target scattering chamber [7]) and an outer radius of 133 mm. To minimize multiple scattering, a unique module design with extra-long 33 cm strips has been developed to reduce the material budget to about 1.4% of a radiation length per region (two silicon planes) for normal incidence tracks, which is essential for tracking at low momenta [8]. No module services, such as cooling lines, power, readout, and slow control cables were placed in the tracking volume. The module dimensions are 41.9 cm × 4.2 cm × 0.39 cm. All of the SVT modules are identical to minimize production costs. There are no overlaps of adjacent modules and the clearance between them is minimal to satisfy the material budget and acceptance constraints.

The modules are mounted between upstream and downstream support rings. For each region, the upstream ring is attached to the cold plate with screws. The upstream support ring provides a mounting surface for the modules on the upstream end of the detector. It also provides a conduction path for heat to be transferred from the modules to the coolant flowing through the cold plate.

The SVT modules are cantilevered off a chilled cold plate, designed to provide mechanical support and to remove heat generated by the electronics, located at the upstream end of the module outside of the tracking volume (see Fig. 2). The cold plate and upstream ring are bolted to the mounting tube that is attached to the insertion cart with the support tube.

The mounting surfaces of the upstream and downstream rings are machined in such a manner as guarantee planarity. The modules in the vertical and near vertical positions provide stiffness to the downstream ring and to a region as a whole. The regions are shifted along the beam axis to match the required angular coverage. The downstream support rings are made from PolyEther Ether Ketone (PEEK) [9].

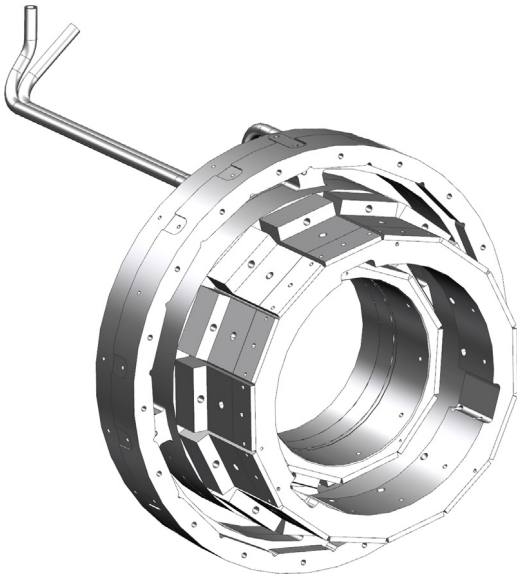

Fig. 2. Upstream support ring attached to the cold plate. The Region 1 and Region 2 heat sinks are shown mounted to the ring.

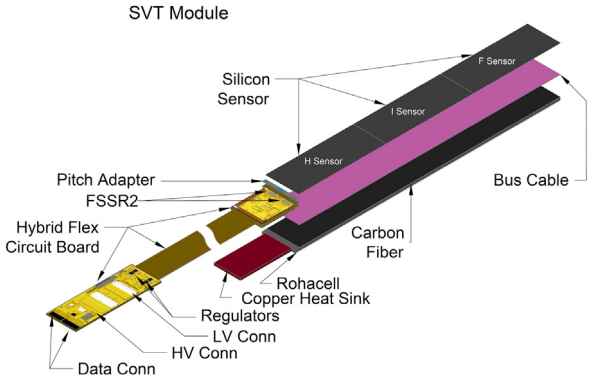

Fig. 3. Layout of an SVT module with the main elements labeled.

Table 1
Electrical specifications of the SVT sensors.

Full depletion voltage	40–100 V
Inter-strip capacitance	<1.2 pf/cm
Leakage current (at depletion V)	<10 nA/cm^2
Strip to backplane capacitance	<0.2 pF/cm
Inter-strip isolation (at 150 V)	>1 GΩ
Resistance of aluminum strips	<20 Ω/cm
Coupling capacitance	>20 pF/cm
Value of polysilicon bias resistor	1.5 ± 0.5 MΩ
Single strip DC current	<2 nA

2.2. Module design

The SVT uses single-sided, 320-μm thick microstrip sensors fabricated by Hamamatsu Photonics, mounted on each side of the module (see Fig. 3). All modules have 3 types of sensors: H (Hybrid), I (Intermediate), and F (Far). The sensors were cut from 6-in wafers with high resistivity of 5 kΩcm to ensure a low full depletion voltage and with 2 sensors per wafer to maximize the yield. The surface damage was minimized by using silicon with a ⟨100⟩ surface orientation. All sensors have the same size, 112 mm × 42 mm. There are three daisy-chained sensors per layer (six per module) with a 110 μm gap between them.

Each layer has 256 strips with linearly varying angles of 0°–3° (constant ϕ pitch of 1/85°) to minimize the dead sensor area. The

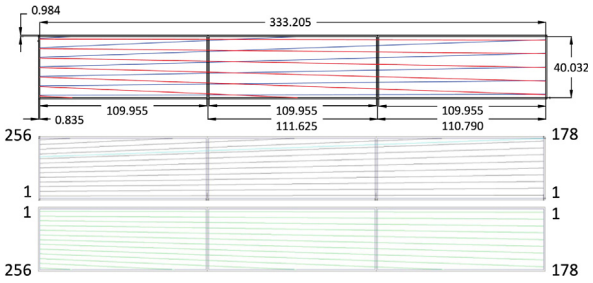

Fig. 4. Sensor strip layout. The hybrid sensor is on the left side. Strip numbers are indicated. Dimensions are in mm.

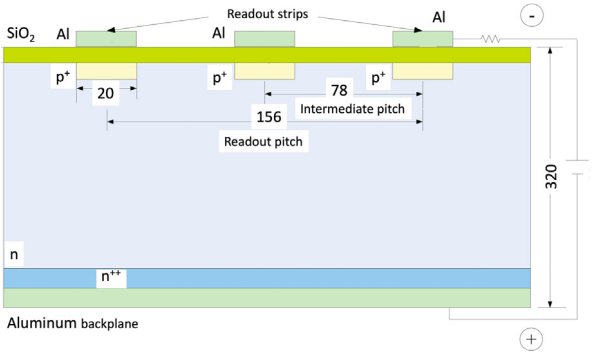

Fig. 5. Cross-sectional view of an SVT sensor showing the different layers and the spacing of the strips (the dimension units are in μm).

first readout strip is parallel to the longitudinal axis of the module; the last readout strip has an angle of 3° with respect to this axis (see Fig. 4). Because of the constant ϕ pitch, the lengths of the readout strips of the modules vary from 0.5 cm to 33 cm. At the hybrid side, the intermediate strip pitch is 78 μm and the readout pitch is 156 μm. It was shown [10] that radiation effects increase the inter-strip capacitance and decrease the backplane capacitance. The strip-to-pitch ratio of 0.256 has been chosen for all three types of sensors, for which the two effects compensate, and the total strip capacitance remains constant with the accumulated dose. Fig. 5 shows a cross-sectional view of the sensor. The aluminum strip width is 26 μm and is AC-coupled via the SiO_2 layer to the 20-μm wide p+ implant strips, which are 1.2 μm below the aluminum strips. The total strip capacitance at 1 MHz is below 1.3 pf/cm and the coupling capacitance is above 10 pF/cm. The electrical specifications of the sensors are shown in Table 1 [11]. The implant strips are grounded via 1.5 MΩ polysilicon resistors. The unpassivated aluminum backplane (ohmic contact) is connected to the positive side of the power supply; the n-bulk volume of the sensor is depleted via the highly doped n++ layer. The guard ring surrounds the sensitive area to reduce the surface currents from the edges of the detector. The 42-mm width of the sensor accommodates 256 readout strips and the 1 mm keep-out zones along the edge of the sensor.

The sensors are mounted on a backing structure designed to provide rigid and lightweight support to the sensors. The backing structure is composed of Rohacell 71 core, 78-μm thick bus cable, and carbon fiber (see Fig. 6). The carbon fiber skin is made from Mitsubishi type K13C2U fibers oriented in a quasi-isotropic (45/−45/0) pattern. To ensure adequate electrical conductivity, it is co-cured with the bus cable, made from a Kapton sheet with 3-μm thick and 0.5-mm wide copper traces; one side provides high voltage (HV) to the sensors, a 6 mm × 6 mm copper mesh on the other side grounds the carbon fiber. The Rohacell core under the hybrid board is replaced by a copper heat sink to remove ∼2 W of heat generated by the ASIC preamplifier chips. At the downstream end of the module, the Rohacell core is replaced

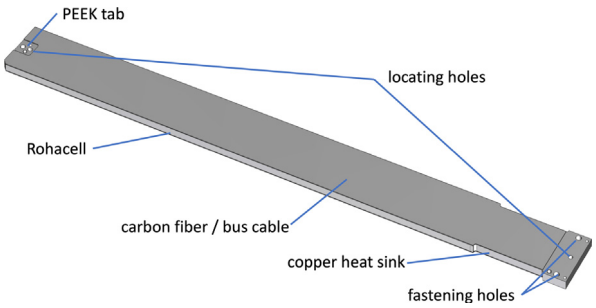

Fig. 6. The module backing structure with the main elements labeled.

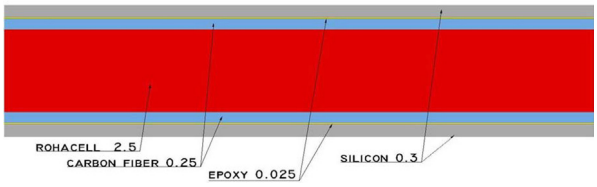

Fig. 7. The cross section of the module. The dimensions are in mm.

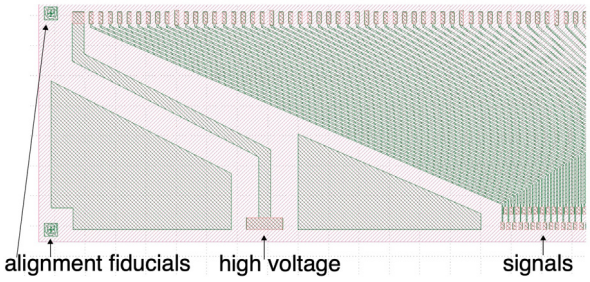

Fig. 8. One end of the pitch adapter mask, showing the alignment fiducials, wire bonding pads, and traces.

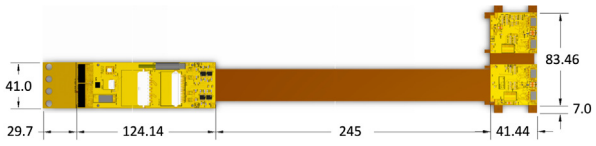

Fig. 9. Hybrid Flex Circuit Board (HFCB). The level one connect board (left side) is connected to the hybrid area (right side).

by a PEEK insert. The cross section of the active area of the module is shown in Fig. 7.

A pitch adapter matches the 156 μm sensor readout pitch to the 50 μm FSSR2 bonding pad pitch. The pitch adapter [12] is a glass plate 41.5 mm × 4 mm (tolerance of 50 μm), with metal traces made of aluminum and copper alloy. The alloy improves electromigration hardness and bonding. The metal layer is sputter deposited. The passivation silicon oxide layer protects the soft aluminum traces from damage. There are two fiducials on the pitch adapter edge next to the sensor and three on the edge next to the hybrid to facilitate alignment. No more than one open trace or two short-circuited traces are allowed per pitch adapter. A section of the pitch adapter is shown in Fig. 8.

Both sides of each module are instrumented with a readout system consisting of a single rigid–flex Hybrid Flex Circuit Board (HFCB) located on the upstream end of the module (see Fig. 9). The HFCB is a single circuit providing all module services and the components to control and read out the signals from the module. The SVT module is attached to the cold plate and all module service cables are passed

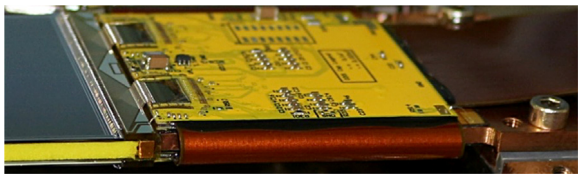

Fig. 10. The wrapping of the HFCB from the top to the bottom silicon layers.

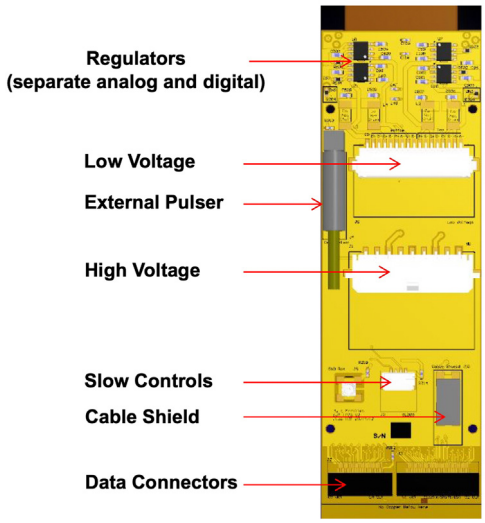

Fig. 11. HFCB level one connect board with the main elements labeled.

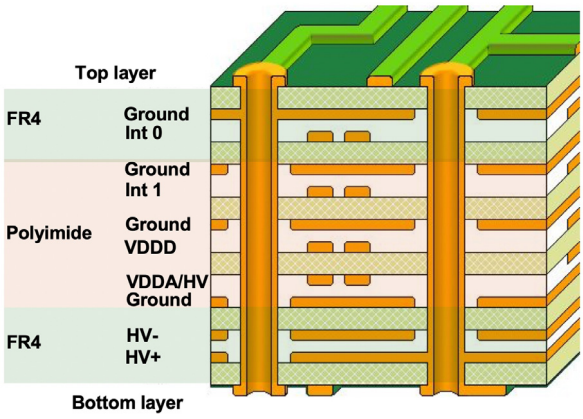

Fig. 12. HFCB 12-layer stack-up.

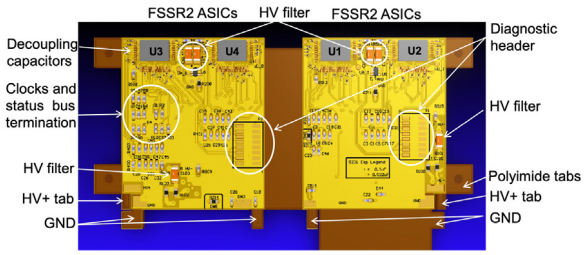

Fig. 13. Hybrid side of the HFCB with the main elements labeled.

through slots in this plate. The design of the HFCB rigid and flex parts accommodates the geometrical constraints imposed by the barrel layout. The HFCB provides bias to the silicon sensors, and power and control lines to four FSSR2 ASICs located at the edge of the hybrid, two on the top and two on the bottom side. The ASICs are glued to pads on their substrates with conductive epoxy. These pads are the reference for the analog return for the chips. The hybrid area of each HFCB (42 mm × 82 mm) consists of two rigid boards (top and bottom hybrids) connected by a 10-mm long wing flex High Density Interconnect (HDI) cable wrapped around the backing structure (see Fig. 10). The transition line from the rigid board to the flex cable was strengthened. Both hybrids connect to the module electrically using micro-bonding technology for the signals and bias return, and solder connections for the detector bias and module support ground. The sensors, the pitch adapters, and the HFCB are glued to both sides of the backing structure.

Module services are provided via the level one connect (L1C) board (125 mm × 41 mm) coupled to the hybrid area via the upstream flex HDI cable (245 mm). The upstream flex HDI cable is routed through 10 mm radial slots in the cold plate. The L1C board hosts two high density Nanonics connectors for data and control lines, a Molex Micro-Fit 9-pin connector for high voltage (~85 V) bias to the sensors, an AMP Mini CT 17-pin connector for low voltage (2.5 V) power to the ASICs, a hybrid temperature connector, an external pulser connector, and four voltage regulators (see Fig. 11). The L1C board is mounted to the support tube on its own support structure designed to keep each L1C board positioned in line with its module.

The HFCB layer stack up (see Fig. 12) consists of six layers of flexible polyimide sandwiched between two triple layers of rigid FR4 (Flame Retardant glass-reinforced epoxy laminate material). The stack up varies from section to section, the flexible sections (wing and upstream flex) only contain the polyimide, whereas the rigid areas contain all 12 layers. This variation in stack up provides the ability to instrument both the top and bottom sides of each module and to pass though the cold plate to the L1C board mounted on the support structure. The two outer layers of the flex stack are the top and bottom shields, which are solid copper pours used to improve signal integrity by providing shielding and references for the differential signals. The top and bottom layers are made from 1 oz copper, while all of the inner layers are made from 0.5 oz copper. The thickness of the rigid boards is 1.42 mm and the thickness of the flex cable is 0.5 mm.

The design of the HFCB reflects recommendations given by the experts in low-noise electronics during the SVT technical reviews. Separate planes are provided for analog (VDDA) and digital (VDDD) power on each side of the hybrid. To reduce noise on these planes, all chip voltage lines are decoupled from the low voltage (LV) return with capacitors near the chips. High voltage filter circuits and the bridging of the high and low voltage return lines are located close to the ASICs (see Fig. 13). Decoupling capacitors for power transmission are placed at the transitions between the flex and rigid materials. All data, clock, status, and register traces (Int0 and Int1) are routed with no crossing of the splits in the reference planes. All clock traces are separated from other differential signals by guard traces that are stitched to the ground planes with vias. The trace width of the guard is 10 mils. No clock signals are routed under the chips to minimize cross talk. All power lines are decoupled from the ground (GND) using 2.2 or 4.7 μF capacitors close to a transition in the printed circuit board (PCB) material (flex to rigid). Sensor bias lines are separated from the data lines by the guard traces. The clocks are terminated at the end of the pair line with two 50 Ω resistors in series between the low voltage differential signal (LVDS) pair, with a 0.1 μF termination capacitor at the node between the resistors and the ground. There are temperature sensors located between the two FSSR2 chips on each side of the HFCB for monitoring purposes. In the hybrid areas, the bottom layer is used to transfer heat from the chips to a copper insert built into the module support core.

Thermal and structural Finite Element Analysis (FEA) on the SVT detector elements was performed using ANSYS [13]. The deflection in the detector was analyzed for an individual module and for a region as a

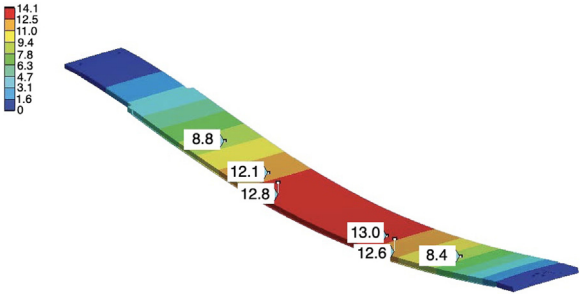

Fig. 14. Deflection of an individual horizontally oriented SVT module due to gravity in μm.

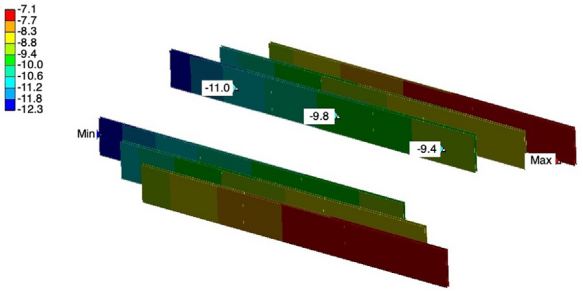

Fig. 15. Temperature distribution along the SVT module in °C.

whole. The deflection was calculated based on the gravitational load on the module. On the upstream end the module was assumed to be fixed since it is fastened to the upstream support ring of the detector. On the downstream end a simply supported condition was assumed since it is supported by the downstream ring. The maximum deflection of a module due to gravity is 14 μm (see Fig. 14) due to the excellent mechanical rigidity of the silicon sensors and the carbon fiber support. The deflection of the downstream ring is less than 7 μm. The vertical modules in the barrel minimize the deflection in the downstream ring making it a fairly rigid structure. The deflection of the entire SVT is 230 μm.

For the thermal analysis, the module was modeled with the copper support and the heat sink insert. The heat output from each module is about 2.5 W. Cooling the cold plate with coolant flowing in the copper tubes that are brazed into the cold plate at −20 °C, at a rate of 2 liters per minute, results in a temperature differential of the coolant between the inlet and outlet of the cold plate of less than 1 °C. The temperature distribution on the module is shown in Fig. 15. The maximum temperature of the sensors at the readout end is −10 °C. The variation in temperature from the upstream end of the Hybrid sensor to the downstream end of the Far sensor is about 1 °C. All components of the cooling system are outside of the tracking volume.

2.3. Module assembly and quality assurance

The position resolution of the detector can be compromised if the sensor alignment offsets are not precisely known. Due to tight material budget restrictions there is no room for an individual module adjustment system. Strict positional tolerances are imposed so that minimal corrections need to be made to the measurements. Therefore, both the position of the sensors with respect to each other and with respect to the alignment points were measured and controlled during module production. A mechanical survey was carried out before electrical testing to check that the module fits within a well-defined envelope and to ensure no interference with adjacent modules on the support structure.

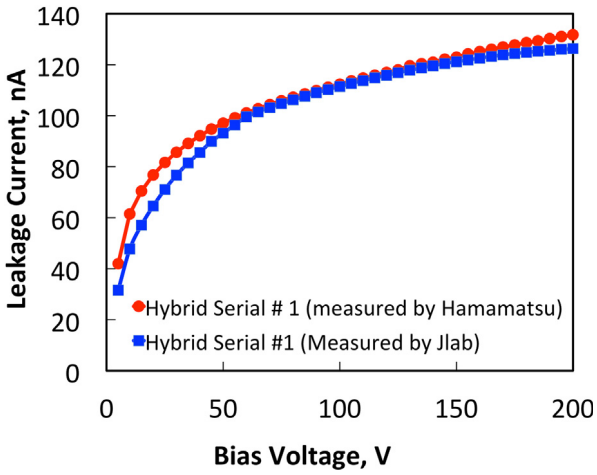

Fig. 16. Typical IV-curve of leakage current vs. bias voltage for a representative silicon sensor.

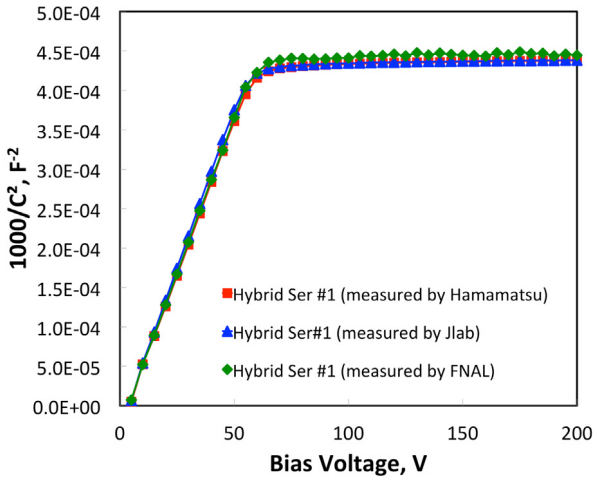

Fig. 17. Comparison of CV plots (capacitance vs. bias voltage) for a representative sensor done by the vendor with measurements at JLab and Fermilab.

The SVT modules were assembled at the Fermilab Silicon Detector Facility and tested at JLab. Prior to installation on a module, all components were inspected and tested as part of the quality assurance (QA) procedure. Risk failure modes were evaluated for all production steps and mitigation actions were taken. A set of detailed assembly procedure documents was developed to aid the assembly work.

Sensor characterization was initially carried out by the manufacturer and later confirmed by the reception testing at JLab and Fermilab. Fig. 16 shows the typical IV-curve for the hybrid-type sensor. The quality of the sensors was excellent. All sensor parameters were better than the specification limits. Sensor leakage currents were well below the limit of 10 nA/cm^2 (470 nA) and there were no defective strips.

The measurements of the full depletion voltage of the sensors were done by testing the dependence of their capacitance on the reverse bias voltage. Fig. 17 shows good agreement of the data obtained at different test facilities. The full depletion voltage data were found to be within the specifications.

The pitch adapters passed visual inspection. Mechanical survey, bond pull test, and trace resistance measurements were performed on the selected pitch adapters.

The initial tests for continuity, shorts, and current draw on the FSSR2 chips were done by TestEdge, Inc on the wafer level prior to the dicing. The yield was ~99%, 8 failures out of 520 chips. A more detailed testing of individual chips after the dicing was performed at

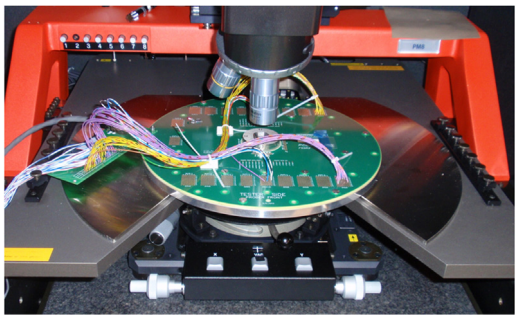

Fig. 18. FSSR2 testing in the probe station.

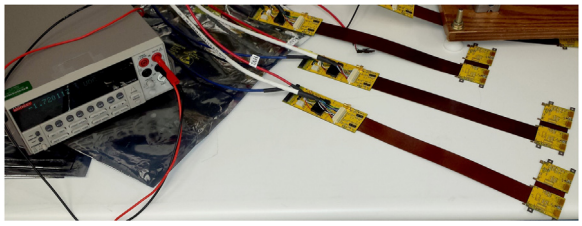

Fig. 19. Electrical test of the HFCBs.

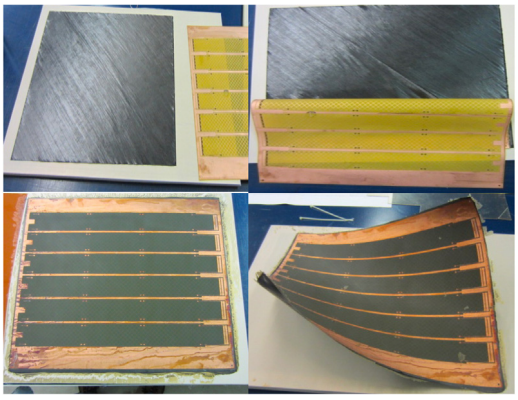

Fig. 20. Bus cable lamination. Top left: preparing the carbon fiber sheet. Top right: placing the bus cable sheet over the carbon fiber sheet. Bottom left: gluing the sheets with epoxy. Bottom right: bus cable skin after co-curing in the oven.

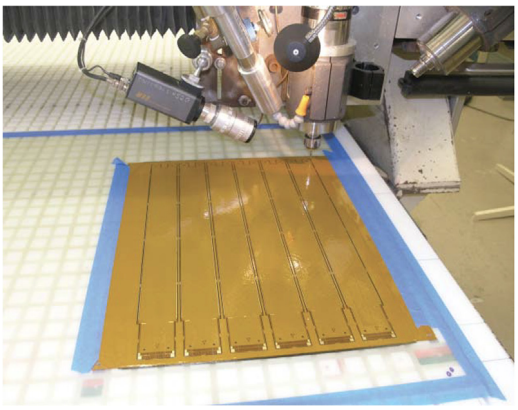

Fig. 21. CNC precision routing of the laminated bus cable skins.

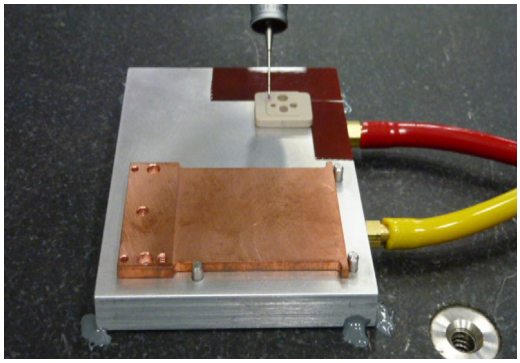

Fig. 22. Inspecting the inserts. The mounting inserts were held on a fixture using its vacuum channels.

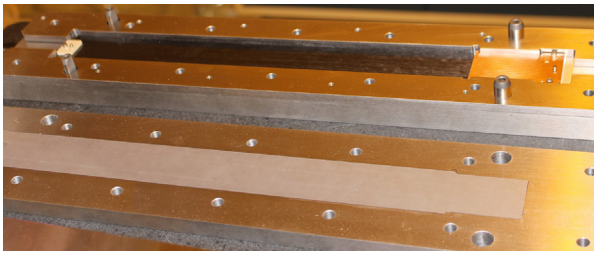

Fig. 23. Assembling the backing structure in the mold.

JLab. Fig. 18 shows the probe card used for the quality assurance of the readout chips. The measurement procedure included register testing (read/write), loading and reading back the mask, measuring channel inefficiency, gain, noise, and threshold dispersion. 330 chips were tested with yield over 90%. No additional dead channels were observed in the modules produced from the tested chips.

Fabrication and primary quality control of the HFCBs were done by Compunetics. A variety of mechanical mock-ups using different 12-layer stack-ups were used to evaluate the bend radius of the wing flex cable. Boards that passed the bending test were sent to the Micro-Craft company for a comprehensive "flying lead" automated electrical testing, including intranet tests for opens, net to net (with 50 mil adjacency) tests for shorts, and isolation tests applying 100 V for 16 ms. HFCB assembly was done by Compunetix Inc. using an automated pick-and-place component mounting system with a thermal profiling reflow system, and automated inspection process. Reception test at JLab included visual inspection, resistance measurements, and burn-in. Acceptance testing of the HFCBs at JLab is shown in Fig. 19.

Fabrication of the backing structure was done in the carbon fiber laboratory at Fermilab. The bottom surface of the bus cable contains a mesh that is used to ground the conductive carbon fiber skins. Since simply gluing the cable to the carbon fiber skin that has cynate ester prepreg does not provide adequate electrical conductivity, to the bus cable panel containing 6 circuits was co-cured into the carbon fiber skin at the same time the lamination was prepared. The panel was laminated on a 3-ply sheet of carbon fiber and co-cured under vacuum in an oven at 120 °C. Fig. 20 shows the process of bus cable lamination to the carbon fiber sheet.

The layout of the six bus cables on a panel has a minimum of 5.05 mm between adjacent cables on the panel to allow for the 1/8-inch diameter routing bit. Fig. 21 shows the process of the Computer Numerical Control (CNC) precision routing of the laminated bus cables. After the routing step, the components of the bus cable (two bus cable skins and Rohacell core) were examined under a microscope and selected for the next fabrication step.

The copper and PEEK inserts were inspected at Fermilab (see Fig. 22). Go/No-Go gauge pins and caliper measurements were done on all inserts. The Coordinate Measuring Machine (CMM) inspection of the precision features was performed on a subset of the parts. A JLab

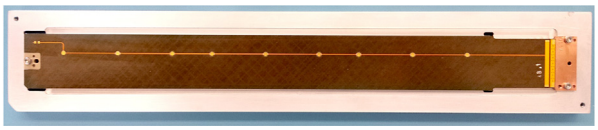

Fig. 24. A fully assembled backing structure.

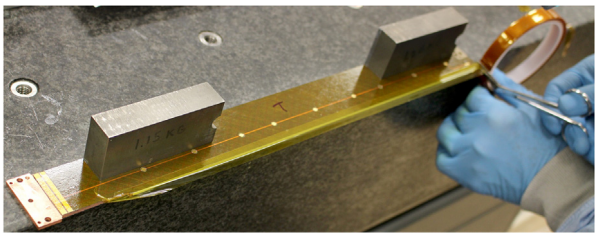

Fig. 25. Insulating the edges of the backing structure.

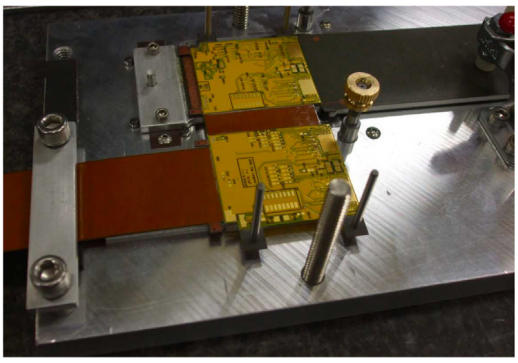

Fig. 26. Fixture for the installation of the HFCB onto the backing structure.

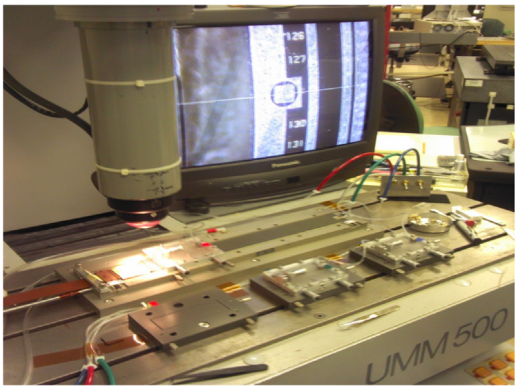

Fig. 27. Sensor alignment in the CMM fixture.

mechanical engineer approved the inspection results before using the inserts in production.

To assemble the backing structure, a mold and an epoxy that cures at room temperature were used (see Fig. 23). Precision pins held the mounting inserts in place. The backing structures were cured on a precision jig to satisfy the required tolerances. The backing structure flatness was within 250 μm.

An assembled backing structure is shown in Fig. 24. Each module has two pairs of mounting and fiducial holes in the copper heat sink (on the right side of the picture) and one in the PEEK insert (on the left side). After a module was fabricated, the positions of these fiducial holes were measured with respect to the fiducial marks etched on the sensor. The copper trace along the backing structure has gold-plated pads to ensure electrical contact from the back side of the sensors to HV bias via silver epoxy applied to them during sensor gluing. There are 3 pads for each sensor. On the right side of the backing structure close to the copper insert, there are wire-bonding pads to connect the HV trace and the copper mesh to the bias and ground pads on the HFCB.

The holes for the mounting pin have a tight diameter tolerance and are used for module alignment. The slot in the PEEK insert has a tolerance of 5 μm. To accurately control the width of the backing structure, post-machining of the width at the downstream end and near the pitch adapter was done. After post-machining of the precision edge, any foam exposed due to that process was encapsulated with 3M DP190 epoxy. The QA procedure for the backing structures included CMM inspection of flatness and precision width, and testing bus cable HV and ground connections. The module dimensions and mounting holes were within the specifications. The edges of the backing structure are covered with Kapton tape to insulate the carbon fiber from the back side of the sensors (see Fig. 25). It was found during testing of the pre-production modules that without the tape, the thin carbon fibers could create a parasitic path from the backing structure ground to the sensor bias contact.

Installation of the HFCB onto the backing structure was done in a special fixture (see Fig. 26). The backing structure was pinned to a base plate with alignments tabs on the HFCB to set its position and alignment of both sides. The bottom side was glued and allowed to cure. The HV and GND tabs were soldered to the bus cable, then the backing structure was flipped over for gluing of the top side of the HFCB, followed by soldering the HV and GND tabs and cutting off the alignment tabs.

Electrically conductive epoxy, Tra-duct 2902, was used to connect the underside of the FSSR2 ASICs to the metallized mounting pad on the board. To place the FSSR2 ASICs in an accurate and repeatable way, a setup fixture was used. The FSSR2 ASICs were located on a base plate and then transferred to the HFCB with a vacuum pickup fixture. The wire bonds on the HFCB, except for those that go to the pitch adapter and the backing structure, were encapsulated with the Dow Corning product Sylgard 186. Visual inspection and electrical testing were done by the JLab staff taking QA shifts at Fermilab.

The backing structure was mounted to a removable support plate on the fixture with an optical CMM. The backing structure with mounted HFCB was attached to the fixture with a clamp. Vacuum channels in the fixture were used to ensure the planarity of the backing structure. A coordinate system was established from the mounting hole and the slot. The alignment frames were used to roughly align the sensors with no epoxy and were then withdrawn. The epoxy was spread on the surface of the backing structure and silver epoxy was applied to the HV pad areas using masks. The sensor alignment frames were moved into place and the final alignment with respect to the insert and sensor fiducials was set (see Fig. 27). The pitch adapters were positioned by hand.

A weight block wrapped in Kapton tape held the sensor during the curing process. Sensor alignment and flatness were within the specifications, and most sensors were aligned to within 5 μm as was validated by the independent sensor alignment survey on the Optical Gaging Products CMM.

After installation of the HFCBs and pitch adapters, the module was placed in a carrier box designed to allow for storage of partially and fully fabricated modules (see Fig. 28). The design of the carrier box provides secure mounting of the double-sided module using the location pins with the screws in the copper and PEEK inserts. The flex cable is secured with a clamp. The module can be powered, cooled (using a passive heat sink), and operated in the carrier box. The carrier box allows access to both sides of the module to facilitate inspection and debugging.

The wire bonding of the backing structure, sensors, pitch adapters, and the readout chips was done on the same fixture that was used for sensor placement. The functionality of the readout was tested after the wire-bonding step on each side. Fig. 29 shows an SVT module

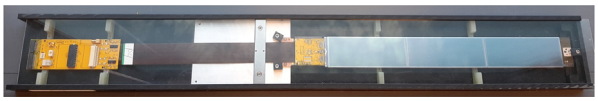

Fig. 28. SVT module carrier box.

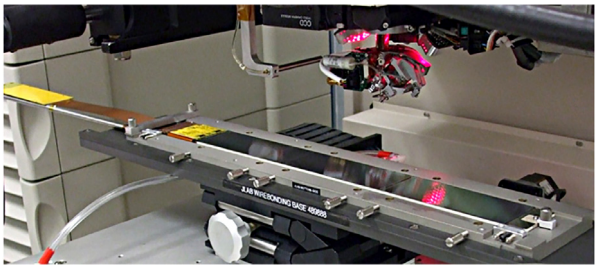

Fig. 29. Wire-bonding of the SVT module.

Fig. 30. SVT modules in the container before shipment.

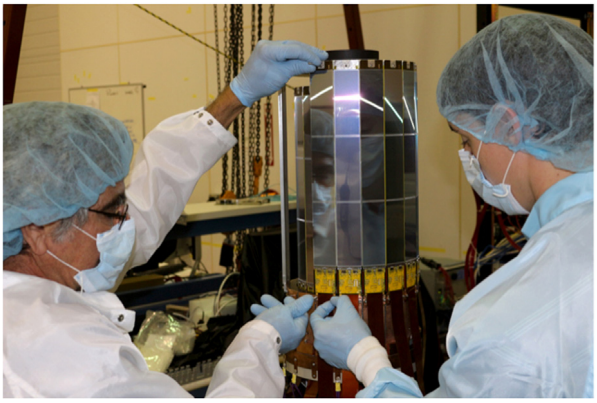

Fig. 31. SVT assembly in progress.

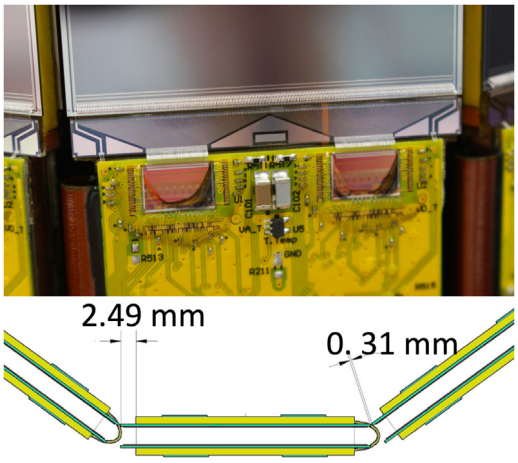

Fig. 32. A close-up photograph of adjacent modules on the barrel (top). Schematic layout of adjacent modules (bottom).

being wire-bonded. Visual inspection of the wire-bonds was part of the module quality assurance procedure.

Module performance tests were done at various stages during module production at Fermilab. A 72-h burn-in test was done on all modules before shipment to JLab. All modules were shipped with the individual travelers containing the part numbers and the survey data for the module components, the results of the quality assurance measurements, and the calibration data. The tested modules were transported to JLab in carrier boxes inside a cushioned container with a shock logger (see Fig. 30), mounted in a wooden crate on shock absorbers. Quality assurance measurements were repeated during the reception test and assembly of the SVT at JLab.

2.4. Detector integration and commissioning

The barrel integration took place at JLab. The regions were assembled in sequence. The assembly was done in a vertical position on a square table with a suspension and leveling system. Positioning the barrel vertically allows access to all modules of the region being assembled and facilitates strain relief of the cables during testing. Region 1 (innermost region) was assembled first, followed by Regions 2 and 3. The modules were mounted on dowels inserted in the support rings by holding the module by the two handling rods that were screwed into the inserts (see Fig. 31).

Fig. 32 shows a close-up photograph and the layout of the adjacent modules on the barrel, demonstrating the two readout chips encapsulated on 3 sides, wire-bonded to the HFCB, the pitch adapter, and the sensor. The sensors extend on both sides of the backing structure by 2.5 mm. The minimum gap between adjacent modules is ~300 μm. The barrel installation procedure was tested successfully, and no modules were damaged during the region integration.

The upstream support ring is fastened to the cold plate by a single screw for each of the copper module supports. This ensures good thermal contact between the inserts on the cold plate and the module supports of the upstream support ring. A layer of thermal compound was applied between the mating surfaces. The cold plate and upstream ring were then mounted to a mounting tube. The large upstream flange on the mounting tube rests on the assembly table (see Fig. 33).

The downstream ring is supported by four aluminum region assembly bars (see Fig. 33) fastened to it to provide stiffness to the ring during assembly. These bars have accurately positioned holes and precision mounting surfaces to position the downstream ring. As the modules are mounted around the polygonal rings, the assembly bars were replaced by the modules one at a time. The mounting surfaces of the upstream and downstream rings were machined simultaneously to reduce twist in the module that could result from the two surfaces not being co-planar. The holes for the locating pins and the tapped holes for the fasteners on the upstream and downstream rings were also added at this stage. Once the downstream ring was in position, a CMM was used to establish a coordinate system and a central axis for the detector based on fiducials machined onto the flange of the mounting tube and the tooling plate on the downstream ring.

The downstream ring has holes in it for accommodating the dowels and screws used for locating and mounting the module on the downstream end. The module has a slot machined into it that accommodates

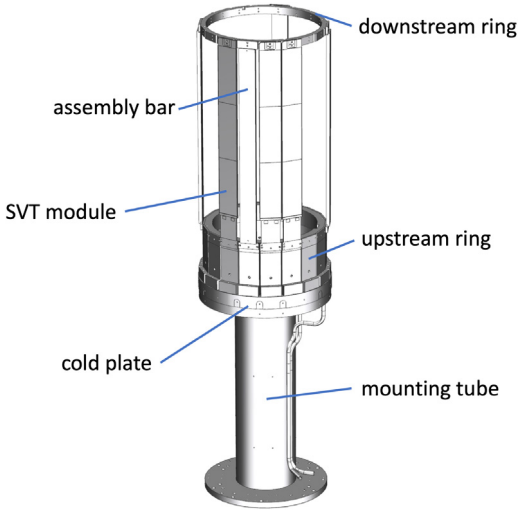

Fig. 33. Region assembly schematic with the main elements labeled.

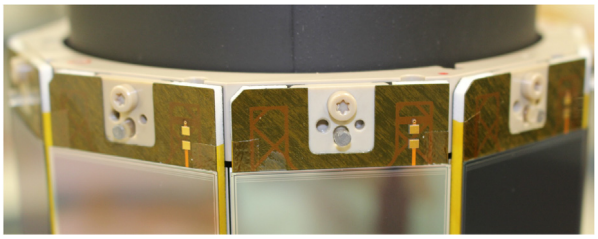

Fig. 34. Close-up photograph of the downstream support of the module.

the locating dowel. This constrains the module in the tangential direction without constraining it in the axial direction. The other holes were used for surveying the module location and for handling the module during assembly. There are three fiducial points on each module, two on the upstream copper insert, and one on the downstream PEEK insert. Fig. 34 shows the inner Faraday cage and the downstream end of the Region 1 modules with the plastic dowels and the screws in the PEEK insert holding the module on the downstream ring. Also seen are the fiducial hole and the screw hole for the mounting rod used to hold the module during installation. The design of the backing structure provided two soldering pads for the surface-mounted decoupling capacitors. The results of the common-mode testing demonstrated that they were not necessary and the capacitors were not installed.

The support rings of each region are independent from each other to prevent over-constraining the assembly. When the inner region was assembled, a light-tight Faraday cage was installed, nitrogen was flushed through it, and the modules were cooled with a portable chiller. The chiller used water as a coolant at a temperature of 10 °C. The process of installing the Faraday cage is shown in Fig. 35. The space between the inner shell of the cage and the Region 3 sensors is only a few mm. A system of 3 aluminum rails was installed on the assembly table to guide the cage over the barrel and to preserve the shape of the carbon shell during the installation.

The barrel was placed in a dark box and tested for functionality and noise performance. Fig. 36 shows the L1C boards of Region 1 attached to the mounting tube with cables connected. The slow controls and the interlock system were in place to protect the SVT during the test.

After confirming the stable operation of the integrated modules, the assembly proceeded with the next region. First, the upstream ring was mounted using the region assembly fixture. The fixture has a mounting ring suspended on vertical rods that can slide in the vertical and horizontal directions. The upstream ring was attached to the mounting

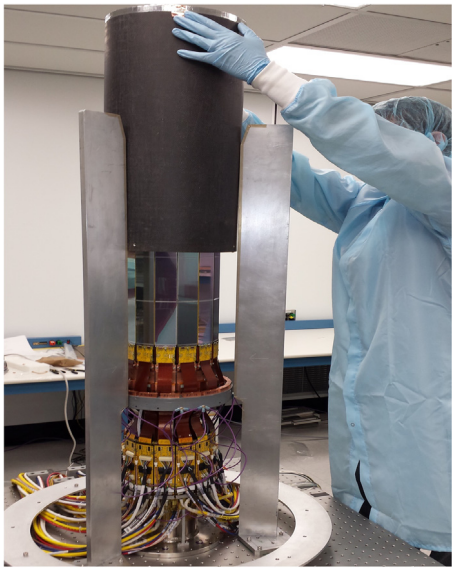

Fig. 35. Installing the Faraday cage of the partially assembled SVT.

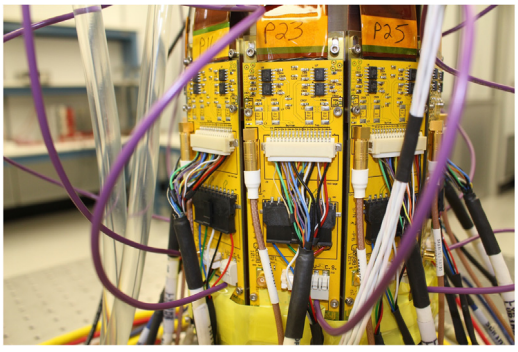

Fig. 36. Close-up photograph of the cable connections during the SVT performance test.

ring, moved on the rails in the fixture, slid over the inner region, and secured to the cold plate with screws. This design allows an entire region to be removed as a unit, rather than module by module. Fig. 37 shows the process of region disassembly. Regions 1 and 2 are still integrated and mounted on the assembly table. Region 3 is removed and placed on a dedicated support structure on the cart.

Upon completion of the assembly of each region, the locations of the fiducials on the downstream and upstream rings were measured with respect to the coordinate axes with a precision of ∼20 μm using a FaroArm Quantum CMM. The displacements between the measured and ideal positions of the fiducials are within a fraction of a mm along the x, y, and z axes, consistent with design tolerances. The fiducial displacement in the xy plane (transverse to the beamline) is shown in Fig. 38. The misalignment shifts of the survey positions from the ideal geometry were taken into account by the alignment software.

After placement of each module on the support structure, all of the modules on the support were re-tested to find and resolve any problems with the cables routed on the outside of the cylinder. Fig. 39 shows the barrel after integration mounted on the assembly bench.

After assembling each region the functionality of the integrated modules was checked. When barrel assembly was complete, it was moved to its transportation cart and rotated to a horizontal position using a special transition fixture. Fig. 40 shows the model of the cart with the SVT barrel mounted on the transition fixture in the vertical and horizontal positions. Fig. 41 shows the process of rotating the

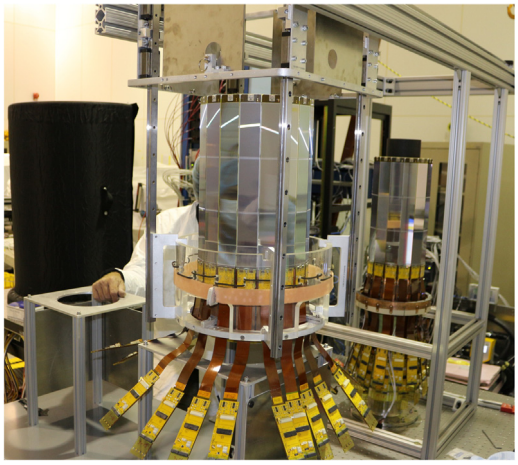

Fig. 37. Region disassembly. Region 3 is in the foreground, removed from the barrel. The integrated Regions 1 and 2 are in the background.

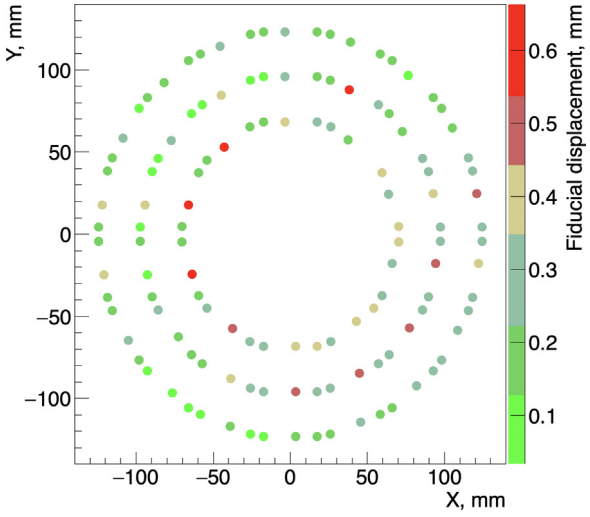

Fig. 38. Fiducial displacements in the transverse xy plane measured in the survey. The z color scale of the plot gives the displacements in mm. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

assembled barrel. Safety locks of the fixture prevented accidental moves of the barrel during the rotation procedure.

The SVT support tube was mounted on the integration cart (see Fig. 42) using a crane and a mounting fixture placed on the parallel rails. The adjustment links on the integration cart and the adjustment plates on the transition cart allow for the SVT to be aligned with the support tube. Fig. 43 shows the attachment of the SVT barrel to the support tube using the transition fixture. The fixture allows fine adjustment of the barrel in the vertical and horizontal directions. The survey of the fiducials on the support structure was performed and the alignment of the barrel was done by shimming the support tube and adjusting the mounting fixture links.

The mounting fixture with attached barrel was moved to one side of the integration cart and locked into place. At this time, all cables and cooling lines were connected to the SVT (see Fig. 44). The cable bundles were secured to the support tube using stainless steel screws and cable ties on the tube and connected to the readout electronics crates.

The detector was tested and commissioned with cosmic rays. The integration cart was enclosed in a protective cover, the wheels were placed in the suspension pods, and the cart was transported to experimental Hall B on a truck. In the hall the SVT was craned off its

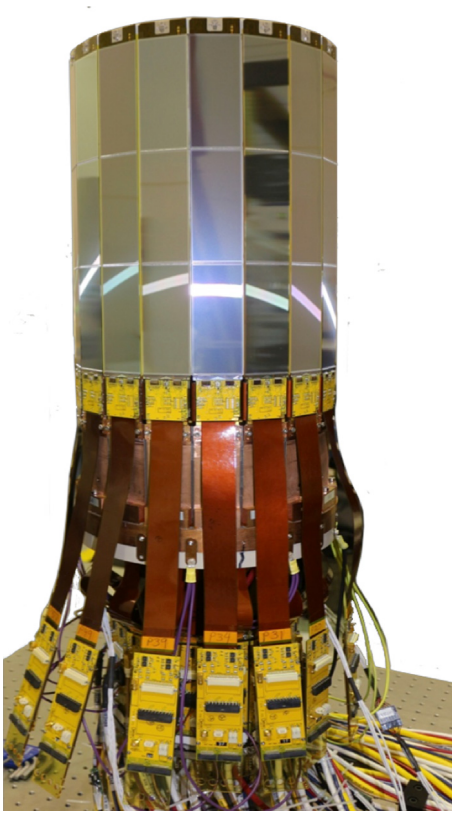

Fig. 39. The fully assembled SVT barrel.

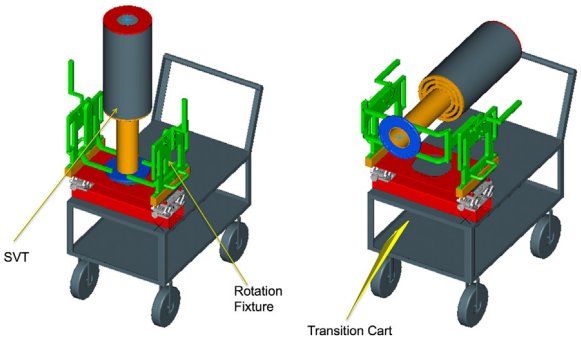

Fig. 40. A computer model of the transition fixture. Left: the assembled barrel is transferred to the fixture. Right: the barrel is rotated, ready to be mounted on the support tube.

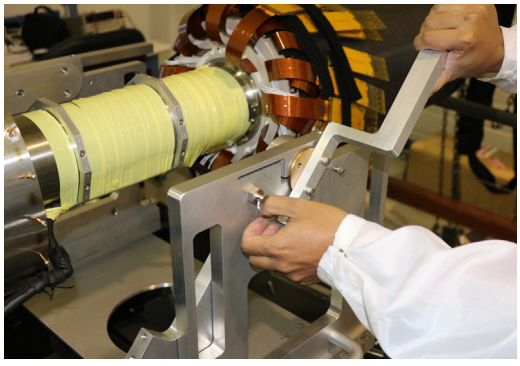

Fig. 41. Rotating the assembled barrel to the horizontal position with the transition fixture. The safety lock is being released to secure the barrel.

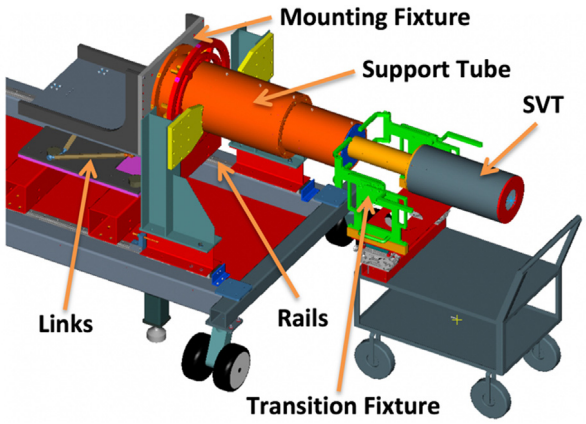

Fig. 42. A computer model of attaching the SVT barrel to the support tube mounted on the integration cart with the main elements labeled.

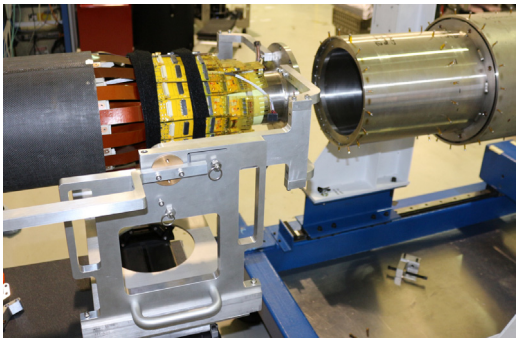

Fig. 43. Attaching the SVT barrel to the support tube.

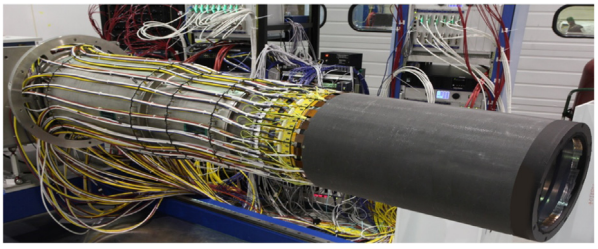

Fig. 44. SVT barrel after integration in the clean room.

integration cart and mounted on its service cart, which hosts all of the detector services and is movable along the beam axis for easy maintenance.

After installation in Hall B, the SVT was tested with the services that are used to operate the SVT during data-taking. A series of runs was performed with and without the beam and with and without the solenoid and torus magnetic fields, four configurations in all. For each of these configurations, the tests of the module performance were repeated. Tests at later stages were aimed at finding problems with the data acquisition and services, such as with the power supplies and cables, in order to ensure that no common-mode noise was added to the system due to improper grounding and shielding.

3. Hardware components and construction

3.1. Cooling and air purging system

The SVT regions are cantilevered off a chilled cold plate that is designed to remove the heat generated by the electronics and to provide

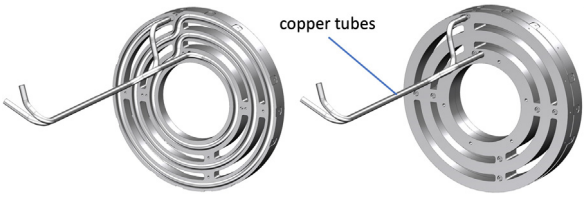

Fig. 45. Copper tubing lines brazed to the copper cold plate (left) and the fully assembled cold plate (right).

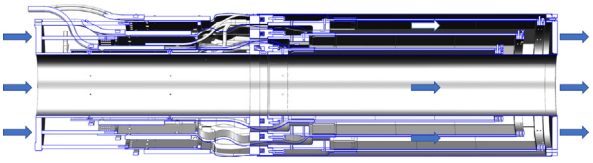

Fig. 46. Cross section of the SVT detector showing the dry air flow past the connectors, through the slots in the cold plate, into the Faraday cage, past the sensors, and out through the holes in the downstream cap.

the required operational conditions for the sensors. External cooling has been chosen over internal cooling (tubes in the modules) to keep the amount of material in the active area as low as possible. The front-end electronics produce about 2.5 W per module, with the 42 total modules producing about 105 W. The HFCB flex cables are routed through 10-mm slots in the cold plate. The cold plate (see Fig. 45) includes a copper plate with brazed copper 0.25-in inner diameter tubes and a PEEK plate on the upstream side. The sensors are cooled by cold air. The coolant lines to and from the cold plate are placed inside of 0.5-in diameter nylon tubes. Air flows inside the 0.5-in tubes, outside the coolant tubes, to cool the air. The air flows out of the 0.25-in tubes through holes in the cold plate, into the sensor area. The chiller pipes were covered with insulating foam to avoid ice formation on them.

Coolant (Dynalene HC50) flows at a rate of 2 liters per minute at a temperature of −25 °C. The cold plate upstream cover is made of PEEK plastic. Dry air flowing through the slots in the cold plate is cooled by the liquid coolant circulating in the tube inside the air purging line (see Fig. 46). With 100 liters per minute of chilled air flow across the cold plate, the sensors are cooled to the operational temperature of −10 °C. The Faraday cage cap on the downstream end has 4 holes to ensure the flow of cold air along the barrel.

The outer shell of the Faraday cage is insulated with a 3-mm-thick neoprene sheet. The barrel is protected from environment humidity by purging dry air between the scattering chamber and the inner shell of the Faraday cage and between the outer shell of the Faraday cage and the protective plastic cover.

3.2. Slow controls and detector monitoring

Ambient conditions inside the detector are monitored by temperature and humidity sensors installed on the upstream rings (see Fig. 47). There are 3 ambient sensor boards glued in dedicated slots on the inner side of the rings in Regions 2 and 3. There are 2 temperature and 2 humidity sensors on each board for redundancy.

Safe operation of the tracker is ensured by Experimental Physics and Industrial Control System (EPICS)-based real-time monitoring of all important operational parameters and status of the hardware components [14]. The software and hardware interlocks continuously monitor the critical system parameters. A multi-level user interface provides safe operation of the SVT by the shift crew and all necessary tools for the system experts (see Fig. 48). Detailed fault charts for the software and hardware monitoring systems were made, and the required actions have been implemented in the interlock system.

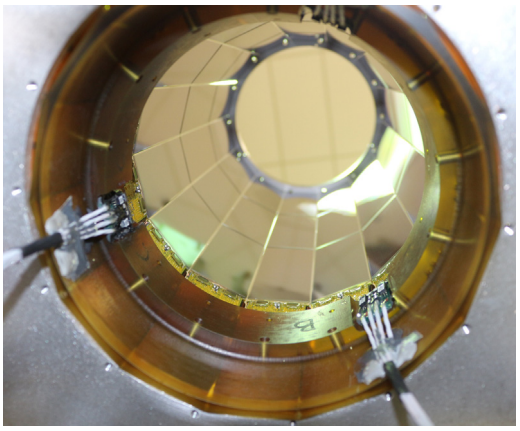

Fig. 47. Ambient sensor boards mounted on the upstream rings.

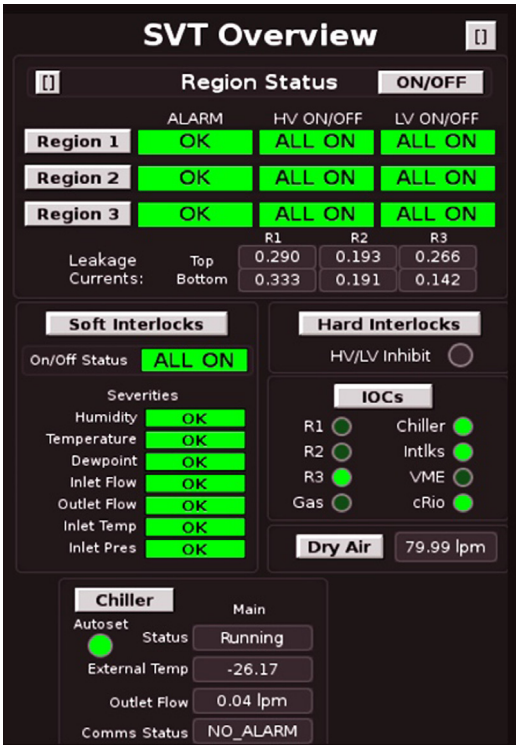

Fig. 48. User interface for the SVT slow controls.

The SVT Hardware Interlock System (HIS) is a backup system designed to protect the detector from damage in case the main control system fails or if network communication is lost. This is a stand-alone system independent from the main EPICS-based slow controls system and does not rely on network communications to safeguard the SVT detector. The HIS is based on the National Instruments CompactRIO (cRIO) Programmable Automation Controller (PAC) platform. The cRIO is a reconfigurable embedded control and acquisition system. The cRIO system's hardware architecture includes I/O modules, a reconfigurable field-programmable gate array (FPGA) chassis, and an embedded controller. The HIS monitors key detector parameters and takes corrective action if a monitored signal is outside of pre-programmed limits. The signals monitored include: HFCB temperature, ambient and detector temperature, humidity, dew point, coolant flow, pressure, temperature, and coolant leak detection (see Fig. 49).

Under fault conditions, the HIS disables the HV and LV crates via the front panel connector on the crate controller. When disabled by the

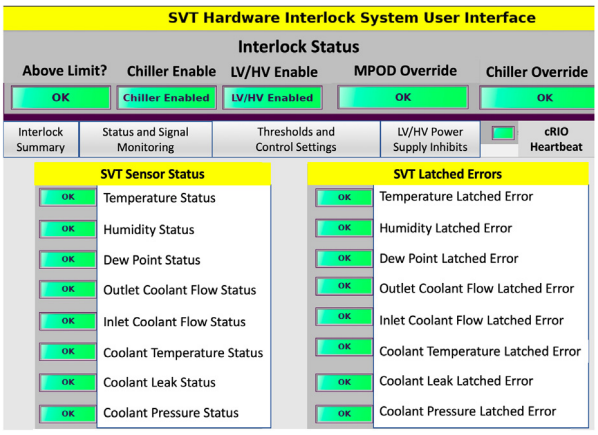

Fig. 49. User interface for the SVT Hardware Interlock System (HIS).

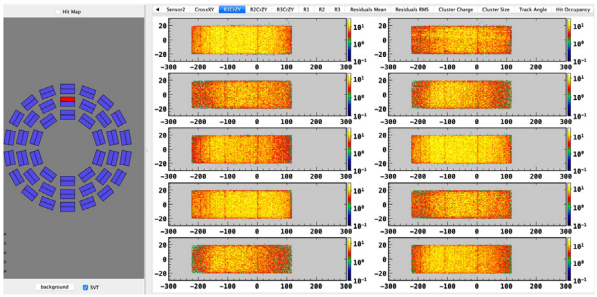

Fig. 50. SVT detector monitoring interface. The SVT layout canvas is on the left side and the right side shows one of the monitoring canvases.

HIS, the EPICS controls are overridden and all channels of the HV and LV crates ramp down at their pre-programmed rate. A reset of both the HIS and the EPICS crate control is needed in order to re-power the HV and LV channels. Under fault conditions, the HIS shuts off the AC power to the SVT chiller.

The HIS is the last line of protection for the detector. If the main EPICS slow controls system works correctly, the HIS should never need to take corrective action to protect the detector. The trip levels for the HIS are slightly outside of the EPICS trip levels to prevent both systems from tripping at the exact same level. The EPICS slow controls system (if working correctly) should always trip before the HIS. The current status of the slow controls and interlocks is reported on the CLAS alarm handler [15].

The front panel of the HIS has two interlock keys. These keys allow system experts to update the cRIO system while the SVT detector is powered. These keys are normally locked in the enabled position during detector operation. The user interface to the HIS allows the operator to remotely monitor the SVT and to set interlock trip levels. The user interface is also used to reset the system after an interlock trip event.

The performance and stability of the system was tested at various operation temperatures. The observed sensor leakage currents remain below 400 nA in normal operating conditions with the coolant at −20 °C. The monitoring of sensor leakage currents is done for each side of the modules (three individual silicon sensors are connected in parallel). Humidity inside the barrel is kept at 2% by purging dry air. All critical detector operational conditions (currents, voltages, ambient sensor readings, interlocks, etc.) are recorded in a MYA database [16] to evaluate system performance and stability. Depletion voltage monitoring is based on the cluster size and cluster charge data taken during the full bias scans.

Java-based data quality monitoring tools were developed to check detector performance both online and offline. The SVT detector monitoring interface is shown in Fig. 50. The tools allow for checking the

status of track reconstruction and performance of the SVT modules. Individual sensors can be selected from the SVT layout canvas on the left side of the interface. On the right side a specific set of histograms can be selected with the tabs. The selected tab shows the position of the reconstructed crosses on the surface of the sensors for the first SVT region. The gaps between the sensors are visible.

4. Electronics

4.1. Grounding and shielding

In a comprehensive noise analysis, different configurations for the grounding were studied to define and validate the final scheme. The signals from the aluminum readout strips are input to the FSSR2 ASIC. The returns of the floating high and low voltage supplies are isolated from the Hall B ground. To maintain the reference voltage level of the carbon fiber, the copper mesh on one side of the bus cable is connected at the hybrid area of the HFCB to the return line of the low voltage. The modules are read out by the FSSR2 ASICs located on the hybrid area of the HFCB and the power and readout connections are made at the L1C. There is no coupling of the power or return lines of different modules — each module is independent of the others. All modules are electrically isolated from the detector support structure. Each crate in the system has a safety ground. To shield against electromagnetic interference, the cable shields – signal, power, slow controls, and pulser – of each module are connected together at the L1C. The L1Cs of all modules are located at the entrance of the Faraday cage, and from each of the L1Cs a cable connects the shields to the Faraday cage, which in turn are connected by a single cable directly to the Hall B central ground (see Fig. 51). The SVT is placed inside a Faraday cage that comprises the cold plate, a forward disk, and a cylindrical carbon shell.

Common-mode noise is of particular concern in digital read-out systems as it cannot be measured on an event-by-event basis and thus a correction is impossible. It can only be estimated statistically. It is important to ensure that the input noise of the modules does not increase with services successively added to the system, as that would indicate problems in the grounding scheme and common-mode noise has been introduced into the system. The analysis of the common-mode noise validated the decisions made on grounding and shielding of the HFCB and the detector. The measured noise levels are in good agreement with the expectations.

4.2. Power supplies

Each side of a module has a high voltage channel, 80 V (40 μA), and two low voltage channels, 2.5 V (0.3 A). To power the FSSR2 ASICs and to bias the modules, Wiener's Universal Multi-channel Low and High Voltage System (MPOD) crates are used. The crates are 19-in tall, rack-mountable, and capable of housing 10 LV Wiener cards or 10 HV ISEG cards, or a combination of the two (see Fig. 52). The output voltage channels of the cards are floating. All power supply channels have programmable voltages, ramp rates, and limits. Hardware limits on voltage and current can be set on each card. Local control of the crate and cards is available on the LCD front panel; remote control is facilitated by a 10/100 Ethernet connection.

For low voltage, the Wiener eight-channel LV cards are used. These cards have a peak-to-peak voltage (Vpp) ripple of 10 mV and are capable of providing up to 8 V at 5 A per channel via a 2 × 37-pin, sub-D connector. Each output channel has a 12-bit voltage setting and measurement resolution, as well as a 12-bit current monitoring resolution. To bias the modules, the ISEG high precision, 16-channel HV cards are used. These cards have a Vpp ripple of 5 mV and are capable of providing up to 500 V at 10 mA via a Redel multi-pin connector. Each output channel has a 21-bit voltage setting and measurement resolution, as well as a 21-bit current monitoring resolution. Clean power, provided by shielded isolation transformers, is used for the HV and LV power supplies. A study of the power supply modules revealed that their contribution to the common-mode noise in the SVT modules is negligible.

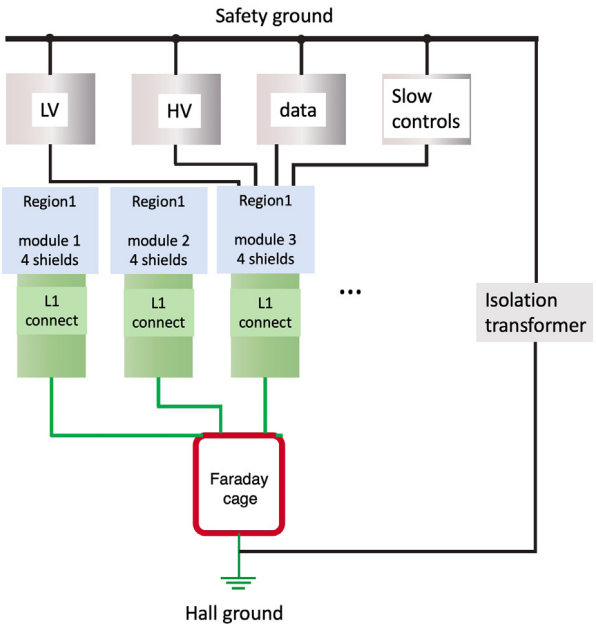

Fig. 51. The SVT grounding scheme.

Fig. 52. Wiener MPOD LX crate with mixed low and high voltage modules.

5. Signals and readout

5.1. Front-end readout electronics

There are 512 channels per module read out by the FSSR2 chips, mounted on a hybrid. The FSSR2 ASIC has been developed at Fermilab for the BTeV experiment [17]. The chip (see Fig. 53) features a data-driven architecture (self-triggered, time-stamped). Each of the 128 input channels of the FSSR2 ASIC has a preamplifier, a shaper that can adjust the shaping time (65–125 ns), a baseline restorer (BLR), and a 3-bit ADC. The period of the clock called the beam crossing oscillator (BCO) sets the data acquisition time. The injected charge causes the discriminator on the selected channel to fire, generating a fast trigger output (GOTHIT) followed by readout of the hit data (OUT1) approximately 1.4 μs after the trigger. The bunch counter clock (BCOCLK) provides the time stamp with which to tag the data.

The analog section of the FSSR core consists of 128 channels (see Fig. 54). The charge preamplifier integrates the input charge generated in the active volume of the sensor with backplane capacitance C_D and collected through the coupling capacitance C_{AC}. The G_f transconductance is used to discharge the feedback capacitance C_f. The integrator and shaper are used to improve the signal-to-noise ratio. Its transfer

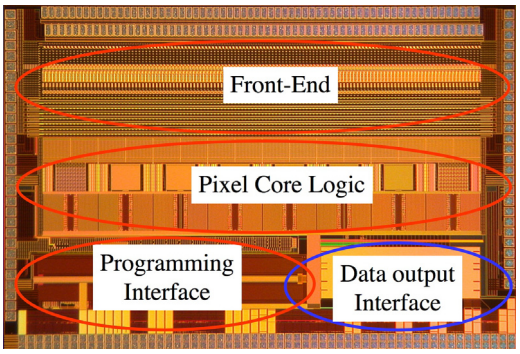

Fig. 53. FSSR2 ASIC with the different functional areas labeled.

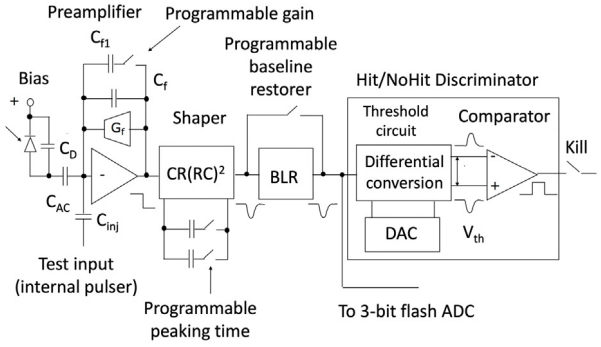

Fig. 54. A block diagram of a single FSSR2 analog channel with the main elements labeled.

function is CR-$(RC)^2$-type with a programmable peaking time of 65, 85, 100, and 125 ns. The comparator provides the binary information (hit/no hit) to the digital section. The BLR is included to achieve baseline shift suppression. It can be bypassed by a programmable switch. The electronics calibration can be performed either by the internal square-wave pulse generator or by an external pulser, providing voltage steps on the integrated inject capacitance C_{inj} of 40 fF. The injected channels can be selected by a programmable inject mask. The gain of the preamplifier is also programmable by changing the value of its feedback capacitance [18].

If a hit is detected in one of the channels, the core logic transmits pulse amplitude, channel number, and time stamp information to the data output interface. The data output interface accepts data transmitted by the core, serializes it, and transmits it to the data acquisition system. Thus, an irregular data flow is converted into data synchronized with the main clock frequency of the system. No time is allotted for transmitting stored information in the FSSR2 working cycle, i.e., the data arrive at the chip output directly after the signal is detected. The signal reception board should be permanently ready for receiving data, since the data can arrive at any moment. Therefore, the chip can operate only as a part of the software — hardware complex with the external controller tuned for the data-waiting mode (time-variable data flow).

To send the 24-bit readout words one, two, four, or six LVDS serial data lines can be used. Both edges of the 70 MHz readout clock are used to clock data, resulting in a maximum output data rate of 840 Mb/s. The readout clock is independent of the acquisition clock. Power consumption is ≤4 mW per channel. The FSSR2 is radiation hard up to 5 Mrad [19]. The choice of the readout chip was driven by its architecture and good noise performance at high capacitive load of the long SVT strips.

The FSSR2 ASIC architecture is such that it sends out 24-bit data words if a channel has a hit or a 24-bit status word if the channel does not have a hit (idle state) within a BCO clock cycle. The FSSR2 ASICs transmit these data over six lines. First, the data are de-serialized. The 24-bit data words are appended with 8 bits to make the time range longer, and the 32-bit words are correlated with the CLAS12 trigger, which is generated by other detectors. The status words are suppressed to minimize the data size of an event. However, the status words are monitored to diagnose the performance of individual FSSR2 ASICs. Each channel has a memory cell for writing a single event. If the data on the event arrive into the cell, the channel is disabled, and the data presence signal is sent into the controller. The controller interrogates the channel with the detected event and produces a data word. The data are transmitted in a short time interval, and, after that, the channel is again ready for receiving signals. Under relatively low rates, when the interval between events is longer than the time required for reading a single event, data losses are absent.

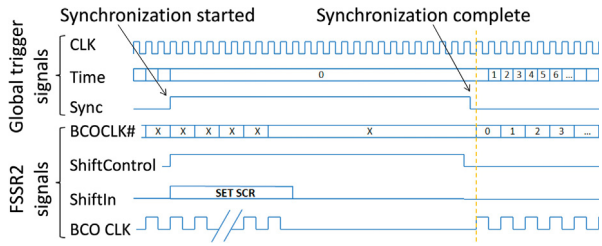

Fig. 55. FSSR2 clock and time stamp synchronization. The BCO clock is halted when SYNC is asserted and started with its rising edge aligned to the global trigger clock rising edge.

5.2. Back-end readout

The four FSSR2 ASICs on the HFCB communicate with the VXS architecture-based Segment Collector Module (VSCM) [20]. The main purpose of the VSCM is to convert the FSSR2 data-driven information stream into the sparsified and triggered events that are correlated with other CLAS12 detectors. The VSCM configures the FSSR2 ASIC registers, provides analog calibration pulses to the FSSR2 ASICs, sets/monitors proper control signals (clock, reset, status), and acquires serialized event data from the FSSR2 ASICs.

Each FSSR2 ASIC has six LVDS pairs with a source synchronous clock to transmit event data. The VSCM supports receiving data from all six LVDS pairs of each FSSR2 ASIC running at 70 MHz double data rate (DDR) (840 Mb/s from each FSSR2). Xilinx Spartan 6 FPGAs are used to buffer and deserialize the data from two FSSR2 ASICs each. Four of these FPGAs are used to support the simultaneous data streams from eight FSSR2 ASICs coming from two HFCB interfaces; the FPGAs in turn send their information to the master FPGA where the event builder resides.

Each VSCM can interface with two HFCBs. Up to 16 VSCM cards can reside in a VXS crate. When multiple VSCM cards are used, additional cards, the Trigger Interface (TI) and Signal Distribution (SD), are required to ensure event and timing synchronization. The VSCM supports a stand-alone mode, useful when only one or two HFCBs are used. The event builder of the VSCM uses the BCO clock time stamp from the data word of each FSSR2 ASIC and matches it to the time stamp of the global system clock, given by the CLAS12 trigger. Fig. 55 shows the timing diagram for the FSSR2 clock and time stamp synchronization.

The global trigger system "CLK" and "SYNC" signals are used by VSCM to phase align the BCO clocks and counters across all FSSR2 chips. When SYNC is asserted, the BCO clock is halted after a smart reset is issued to the FSSR2. When SYNC is released, the BCO clock is started with its rising edge aligned to the global trigger clock rising edge. The FSSR2 ASIC data is tagged with a global trigger time stamp (48 bits, 8 ns resolution). Since the BCO clock is derived from the global system clock, triggers received by the VSCM will cause the

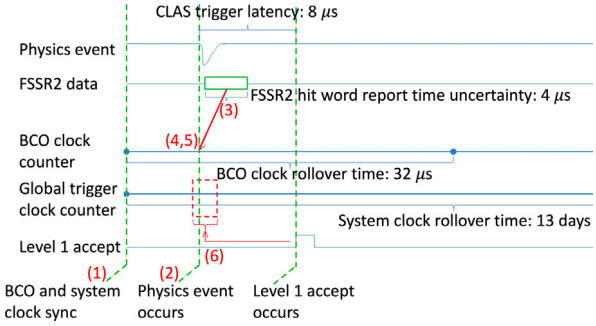

Fig. 56. VSCM event triggering. See text for description of the sequence.

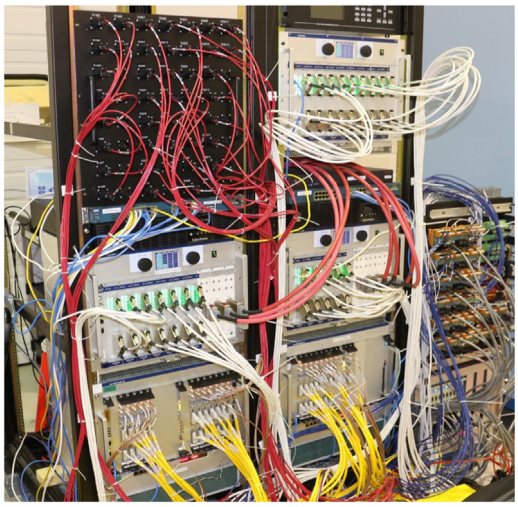

Fig. 57. The SVT test stand installed in the clean room.

event builder to extract only the hits with specific BCO timestamps that correspond to a programmable time window where the physics event could have occurred. When a trigger is received, the data words from the FSSR2 ASICs are copied to an event buffer and pushed into an event FIFO. These events can be read out in order with other modules in the system while event-level synchronization across all modules in the system is maintained.

The VME interface provides for event readout, access to the configuration registers on the VSCM, bridges access to the registers of the FSSR2 ASICs, and provides an interface to the CPU. The 32-bit address space, 2 MB in size, is dedicated to the event builder FIFO, which can be read using single-cycle and block transfer VME protocols. Block transfer protocols are used for event readout; the 2eSST protocol used is to maximize performance. The 2eSST protocols provide ~200 MB/s sustained transfer rate and supports the proprietary JLab token-passing scheme that allows a single direct memory access (DMA) operation on the CPU to transfer data from all VSCM modules sequentially, eliminating overhead (compared to individual board transfers). The VSCM is set up to extract event data within a programmable look-back window of ~16 μs relative to the received trigger.

The VSCM design makes the FSSR2 data-driven architecture compatible with the CLAS12 free running data acquisition system (DAQ) [15]. Fig. 56 describes the VSCM event triggering. At (1) a system reset and synchronization is performed. A physics event occurs at (2). At (3) the FSSR2 time unsorted hits arrive. At (4) the VSCM tags hits with the global trigger counter using the BCO number. The VSCM stores hits in the FIFO by the strip number at (5). At (6) level 1 accept received the FSSR2 hits with the global trigger counter matching the trigger window. The VSCM can handle large detector occupancies.

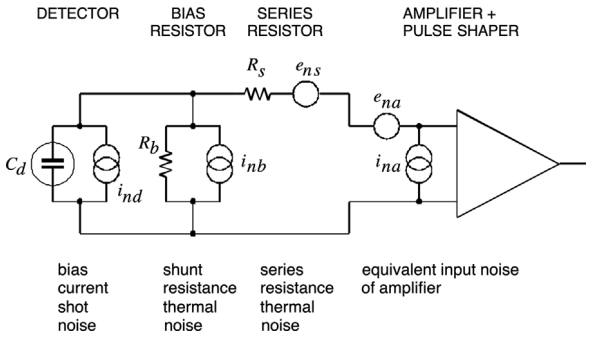

Fig. 58. Equivalent noise circuit diagram. Serial noise sources are shown as voltage sources and parallel sources as current sources.

The calibration pulser circuit provides a 2 Vpp dynamic range, up to 125 MS/s, and 14-bit resolution (for pulse height steps in sub-mV increments). The bandwidth is sufficient to allow 10 ns rise times to be delivered over 15 ft of 50 Ω coax cable terminated into 50 Ω. Two independent pulser outputs are provided to drive both HFCB modules. The pulser signal phase can be placed in a deterministic phase relationship to the BCO clock that drives the FSSR2 ASIC.

During the SVT integration and testing a full-featured test stand (see Fig. 57) accommodating production services (power supplies, DAQ, slow controls, alarm handler, purging, and cooling system) for the whole detector was installed in the clean room.

5.3. Expected noise performance

The sensor thickness and total length of the strips (33 cm) are defined by the technical requirements on the detector acceptance and energy spectrum of the registered tracks. The signal generated in 320 μm sensors is about 24,000 electrons, which makes it essential to minimize all sources of noise and to control the cross-talk.

The equivalent circuit diagram of a silicon strip sensor with connected readout electronics is shown in Fig. 58 [21]. A single channel (3 daisy-chained strips) with capacitively coupled readout is represented by its total capacitance C_{tot}, a coupling capacitance C_c, the resistance of the connection line to the amplifier R_s, the bias resistor R_b, and a filtering capacitance of the bias circuit C_b. The SVT sensor measures the charge deposited by the particles, thus the noise is quoted in terms of the Equivalent Noise Charge (ENC), defined as the charge that, if injected in the input, gives a signal-to-noise ratio of 1. All the noise sources of a circuit can be summarized and represented by a noise voltage v_{ni} appearing on the input of the amplifier. The internal capacitance of the amplifier C_i is connected in parallel to C_{tot}. The dependence of the ENC Q_n on the input capacitance can be parameterized as [22]:

$$Q_n^{RMS} = a + C_{tot} \cdot b, \tag{1}$$

where $a = v_{ni}^{RMS} \cdot (C_f + C_i)$, $b = v_{ni}^{RMS}$, and C_f is the feedback capacitance of the amplifier.

Parallel shot noise from the reverse bias current I_b through the strip can be expressed as:

$$\frac{1}{q_e}\frac{e}{\sqrt{8}}\sqrt{2q_e I_b \tau} \approx 108 \cdot \sqrt{I_b\ [\mu\text{A}]\tau\ [\text{ns}]}, \tag{2}$$

where q_e is charge of the charge carriers and τ is the characteristic shaping time.

Parallel noise from shunt resistance R_b is:

$$\frac{1}{q_e}\frac{e}{\sqrt{8}}\sqrt{\frac{4kT}{R_b\tau}} \approx A \cdot \sqrt{\frac{\tau\ [\text{ns}]}{R_b\ [\text{M}\Omega]}}, \tag{3}$$

where k is the Boltzmann constant, T is the temperature, and A is the temperature-dependent factor equal to 24 at 20 °C and 22.5 at −10 °C.

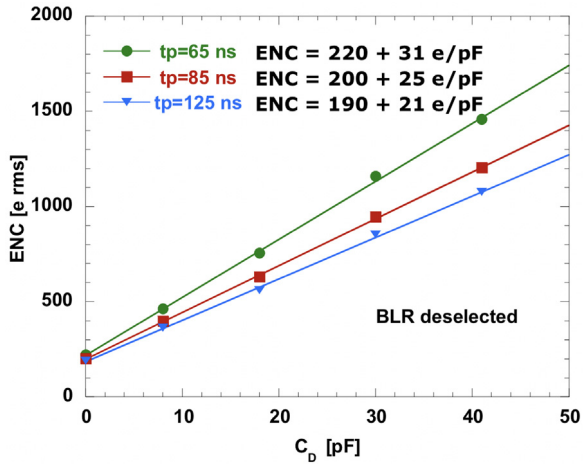

Fig. 59. FSSR2 ENC vs. detector capacitance at different shaping time settings.

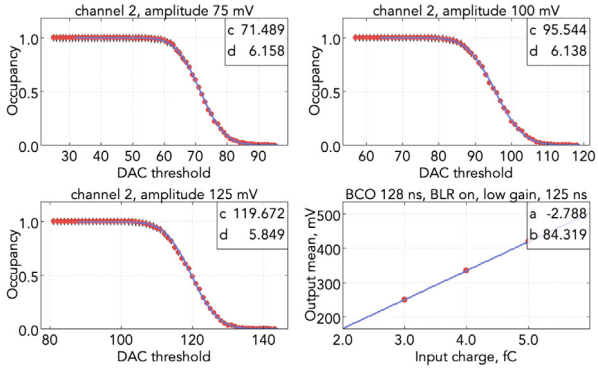

Fig. 60. Threshold scan on a single representative SVT channel. Three occupancy plots taken at different pulser amplitudes and the response plot (lower right) are shown. The parameters results of the $erfc$ and linear fits are shown on the plots.

Series noise from the metal strip resistance R_s is:

$$\frac{1}{q_e}\frac{e}{\sqrt{8}}\sqrt{4kT\frac{R_s}{3\tau}C_{tot}} \approx B\cdot C_{tot}[\mathrm{pF}]\cdot\sqrt{\frac{R_s\ [\Omega]}{\tau\ [\mathrm{ns}]}}, \tag{4}$$

where B is the temperature-dependent factor equal to 14 at 20 °C and 13 at −10 °C.

For non-irradiated sensors the shot noise from the measured sensor reverse bias current 0.05–0.4 μA (256 strips) at −10–20 °C is within 20–50 electrons with a shaping time of 125 ns and can be neglected. As demonstrated in Eqs. (3) and (4), the detector noise does not change much when the sensors are cooled to −10 °C. The contribution from the shunt resistance is about 200 electrons with a shaping time of 125 ns. The total capacitance of the strip C_{tot} including the wire bonds and the pitch adapter is ∼45 pF. The metal strip (33 cm) resistance is ∼230 Ω, which gives an estimate for the series noise of ∼850 electrons.

Fig. 59 shows the results of the FSSR2 noise measurements performed on a single-chip test board with discrete capacitors connected to the amplifier, confirming linear dependence of the noise on the total capacitive load of the amplifier in Eq. (1). The contribution from the amplifier itself is the dominant source of noise, mainly caused by shot noise and thermal noise on the current path of the transistors. Adding all sources of noise gives an estimate for the total ENC for an SVT channel of ∼1500–1600 electrons.

6. Calibration

Since the SVT modules are designed with a binary readout system, the analog channel response cannot be measured directly. Instead, the analog response is reconstructed by injecting a calibration charge on the channel and measuring the corresponding occupancy over a range of threshold values.

The output signals from the FSSR2 chip can be converted to charge using either internal or external calibration pulses. Because the external pulser can be set to a higher frequency than the internal pulser without affecting the calibration process, the external pulser circuit was added to the HFCB and the VSCM. Noise is measured using external calibration charge pulses injected at low frequency in the absence of signal. The injected charge is shaped and amplified in the analog circuitry to form an output signal. The voltage at the input of the discriminator is measured over a certain number of triggers and the discriminator threshold determines whether or not the output signal corresponds to a hit. The probability that the injected charge produces a hit depends on the setting of the discriminator threshold. The average hit probability is measured by repeating the process of injecting charges and counting the fraction of readout triggers that produced a hit. This measurement is repeated over a range of threshold settings to produce an occupancy plot.

The noise occupancy plots are produced by setting the pulser amplitude at fixed values and changing the comparator thresholds. Each point of an occupancy plot for a fixed value of injected charge represents the percentage of time that the comparator fires for a certain value of the threshold settings. In Fig. 60 three occupancy plots taken at different pulser amplitudes for a single channel are presented. The noise occupancy as a function of threshold in case of Gaussian noise is fit by the complementary error function and the probability p of surpassing a threshold τ is given by Eq. (5).

$$p(\tau) = \frac{1}{2}erfc\left(\frac{\tau}{\sqrt{2}\sigma}\right), \tag{5}$$

where σ is the standard deviation of the Gaussian distribution. In the presence of the calibration signal, the occupancy plot shifts to higher threshold values proportionally to the calibration amplitude.

In between the high and low threshold regions, the occupancy histogram for each SVT channel is well described by an error function, or S-curve, producing a mean value (discriminator threshold) and standard deviation (noise). The parameters for the mean and σ of the $erfc$ fits are shown. The conversion to mV is performed considering the width of one DAC bin (3.5 mV). The injected charge is calculated using the nominal value for the FSSR2 injection capacitance of 40 fF. The threshold at 50% occupancy is plotted against the input charge, resulting in a response curve, of which the slope is called the gain G, measured in mV/fC. The response plot shows the linear dependence of the output pulse height on the input charge in the operation region of the preamplifier. The middle point corresponds to the charge deposited in the sensor by a minimum-ionizing particle (MIP). The slope and the offset parameters of the linear fit are shown. The input noise is obtained by dividing the output noise by the gain using:

$$ENC[e^-] = 6242[e^-/\mathrm{fC}]\frac{\sigma\ [\mathrm{mV}]}{G\ [\mathrm{mV/fC}]} \tag{6}$$

The threshold charge must be the same across the channels in the detector, otherwise the track-finding algorithms [23] would be biased by the potential extra hits. Any spread in the response among the different channels of a chip results in a spread of the efficiency and noise occupancy that degrades the effective performance. This leads to a requirement that the channel-to-channel variations in threshold and noise are kept to a minimum. Threshold dispersion is defined to be the standard deviation of the distribution of means obtained from the parameters of the complementary error function fit.

The noise for each individual detector channel is measured and the values are used by the zero-suppression algorithms implemented in the core logic of the FSSR2 and by the calibration procedures to

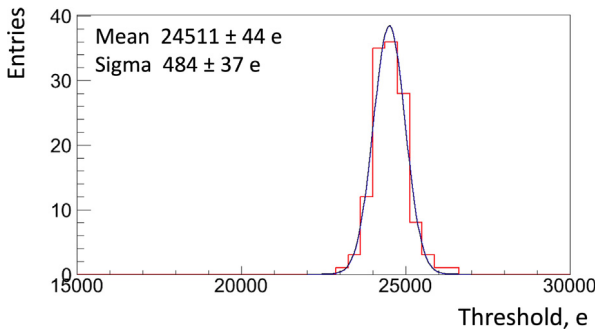

Fig. 61. Typical threshold dispersion within an FSSR2 ASIC chip.

identify defective channels. A comparison of the noise for the 33 cm strips demonstrates that the threshold spread is negligible compared to the noise and does not affect the efficiency and noise occupancy (see Fig. 61). The threshold dispersion agrees with expectations for the FSSR2 chip for the chosen settings.

The SVT calibration parameters are stored in the CLAS12 calibration database (CCDB) [23]. The channel calibration table has columns corresponding to sector, layer, chip identifier, mean, channel status (good, noisy, open, dead, or masked), ENC, gain, offset, V_{t50} (threshold at 50% occupancy), and the threshold. There are 21,504 rows in the channel calibration table. The ENC and gain are calculated using a calibration amplitude equal to 100 DAC counts (injected charge 4 fC). The chip calibration table has columns corresponding to layer, sector, chip identifier, ENC (electrons), gain (mV/fC), offset (mV), the threshold at 50% occupancy (V_{t50}, mV), threshold dispersion (electrons), chip gain (low, high), BLR mode (off, on), BCO time (ns), shaper time (ns), 8 ADC thresholds in DAC. There are 168 rows in the chip calibration table.

7. Local reconstruction

The extraction of signals is done with a threshold set based on the signal-to-noise ratio. A hit is created when a pulse height on a channel exceeds a certain signal-to-noise ratio. To account for particle hits with signals shared by adjacent channels due to capacitive coupling, when the signals of neighboring strips exceed a threshold, they are added to the cluster. The number of strips in a cluster is called cluster size or cluster strip multiplicity. In a binary readout system, where the position information is derived from the strip with the highest pulse height, the root mean square of the spatial resolution is given by the readout pitch divided by square root of 12. FSSR2 is a binary chip and the 3-bit ADC is provided for the calibration purposes. Although the precision of the digitized pulse height is poor, it is still possible to use this information in the reconstruction to improve the spatial resolution compare to binary signal processing. The cluster position is determined from the centroid of the signal amplitudes by a center-of-gravity method using charge sharing between neighboring strips due to capacitive coupling. See Ref. [23] for more details on the SVT reconstruction.

8. Simulation

8.1. Detector simulation

A series of Monte Carlo simulations have been used to calculate the acceptance of the CLAS12 Central Detector and to study the reconstructed physics parameters for the types of events that are of interest. A realistic model of the SVT has been developed, describing the location and composition of all modules, with a material description based on the engineering drawings and assembly procedures, and confirmed by the survey measurements during integration. The SVT design and module layout were validated by Geant4-based simulated

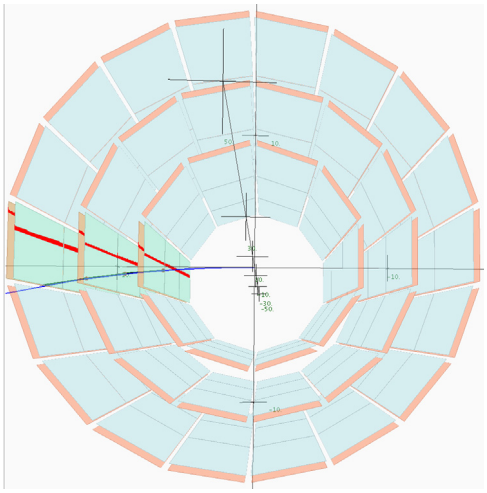

Fig. 62. 3D view of the simulated SVT detector geometry looking downstream along the barrel.

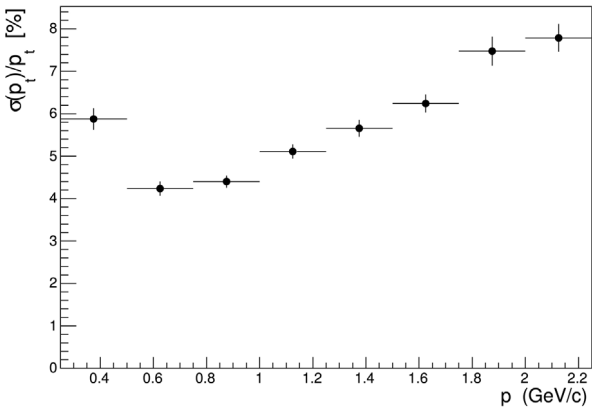

Fig. 63. Simulated SVT momentum resolution in terms of $\sigma(p_t)/p_t$ (transverse momentum) vs. momentum.

detector performance studies demonstrating compliance with the technical requirements and engineering models. A 3D view of the simulated geometry of the SVT sensors is shown in Fig. 62. The SVT model is described in Ref. [24].

According to the results of the simulation of the SVT, a resolution of 50 μm in the bending plane is required in order to measure, with a precision of better than 5%, tracks with momentum up to 1 GeV (see Fig. 63) [25,26]. At low momenta the degradation of the resolution is caused by multiple scattering.

The centroid residual distribution for the simulated muon tracks generated in the interval 0.5–2 GeV is shown in Fig. 64. The cluster centroids were calculated based on the charge-weighting method. The spatial resolution of the sensors in the transverse plane using the ideal SVT geometry with no misalignments was found to be about 30 μm.

8.2. Backgrounds, energy deposition, dose rates

Radiation-induced bulk and surface detector damage studies have been conducted with charged hadrons, leptons, neutrons, and γ-ray photons. The damage can be due to ionizing radiation, affecting the surface, and non-ionizing energy loss from the hadrons interacting with the sensors and introducing lattice defects. The new energy levels within the band gap lead to an increase of the leakage currents, charge trapping that influences the charge collection efficiency and depletion voltage, and changes of the effective doping concentration.

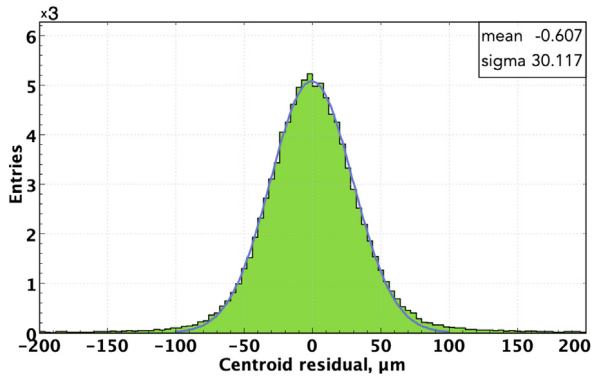

Fig. 64. Simulated centroid residual distribution for the SVT module.

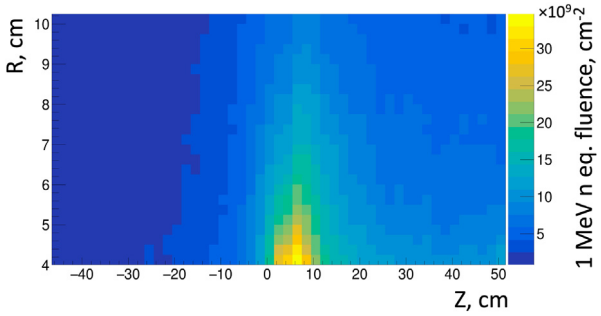

Fig. 65. Accumulated 1 MeV equivalent neutron fluence for a 140-μm-thick lead target. R is the radius, z axis is along the beamline.

The surface damage affects strip isolation and leads to lower position resolution. The bulk damage may occur in point-like and cluster-like shapes depending on the type and the energy of the particle. Protons and pions are more likely to introduce point-like defects below a transferred momentum of 5 keV. The lower threshold to produce a single point defect is ∼25 eV [27]. Neutrons interact only via the strong force, damaging the lattice and creating isolated cluster defects. The radiation damage produced by different particles with different energies is scaled under the assumption of the Non-Ionizing Energy Loss (NIEL) hypothesis as the radiation damage in the silicon bulk depends only on the non-ionizing energy loss. The damage caused by different particles is referenced to the damage from 1 MeV neutrons. The standard value for the NIEL of 1 MeV neutrons is 95 MeVmb. This unit is taken in order to compare different particle energies and interaction mechanisms following the NIEL damage law.

To estimate the expected particle fluence and calculate the effects of different target configurations on the SVT detector, FLUKA [28,29] simulations have been performed. With the help of this tool, the radiation level in the CLAS12 Central Detector can be visualized. In order to include hadron electro-nuclear production, a dedicated source term has been used to enhance the physics production from the target, since it is of key importance in radiation estimates for targets with radiation length below 4%. To assess the radiation damage to the SVT, the accumulated 1 MeV neutron equivalent fluence has been recorded corresponding to the planned run conditions.

For the experiment with the lead target, the expected exposure was 240 h at a beam current of 38 nA with an electron beam energy of 6.6 GeV (see Fig. 65). For a liquid-deuterium target, the study has been done for the accumulated charge of 108 mC at 11 GeV (see Fig. 66). The target is at the point $(R, z) = (0, 0)$. The innermost SVT layer is located in z (along the beamline) from −22cm to 12 cm (the center of the target is at $z = 0$) at a radius $R = 6.5$ cm. The maximum fluence on the sensors depends on their position in the tracker. In both scenarios

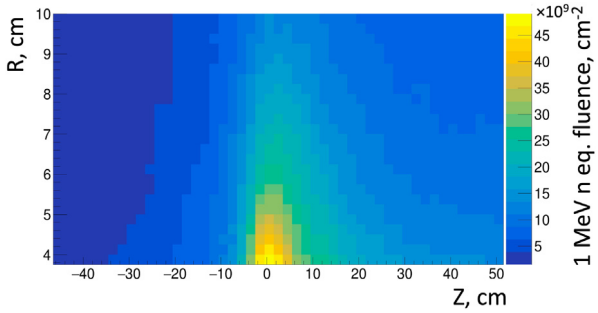

Fig. 66. Accumulated 1 MeV equivalent neutron fluence for a 5-cm-long liquid-deuterium target. R is the radius, z axis is along the beamline.

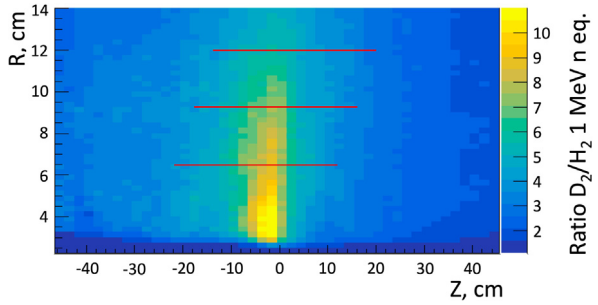

Fig. 67. The ratio of 1 MeV equivalent neutron fluences for a 5-cm-long liquid-deuterium and liquid-hydrogen targets. R is the radius, z axis is along the beamline.

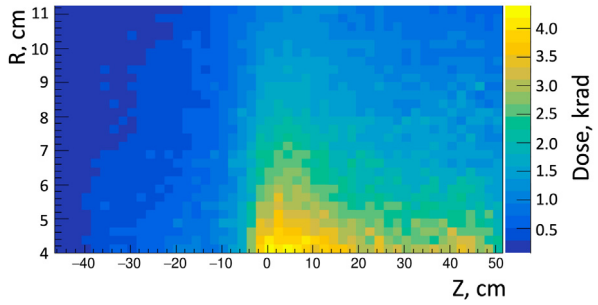

Fig. 68. Accumulated radiation dose for a 5-cm-long liquid-deuterium target. R is the radius, z axis is along the beamline.

the expected doses should not cause substantial degradation of the silicon sensors. Fig. 67 shows the ratio of 1 MeV equivalent neutron fluences for a 5-cm-long liquid-deuterium and liquid-hydrogen targets. The location of the SVT sensors is indicated by the horizontal lines. The difference in the estimated fluences comes from the flux of neutrons produced in the liquid-deuterium target. The largest dose is expected in the intermediate sensors of Region 1.

FLUKA simulations of radiation dose have been performed also in terms of high-energy hadron equivalent fluence that is proportional to the rate of Single Event Effects (SEE) [30]. Hadrons, neutrons, photons and electrons are implemented depending on their spectra. Fig. 68 shows the accumulated dose for a liquid-deuterium target in the same conditions. The rate of the SEE should not cause issues with readout electronics.

Estimated levels of radiation damage in terms of 1 MeV equivalent neutron fluence in silicon in the radial direction are presented in Fig. 69 for liquid-hydrogen and carbon targets at nominal beam currents. Also shown are the radiation levels for the tagger magnet yoke during the beam tuning [7].

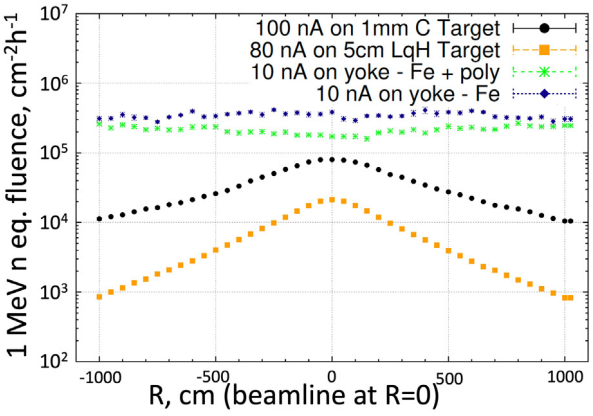

Fig. 69. Estimated levels of radiation damage in the radial direction in terms of 1 MeV neutron equivalent fluence in silicon.

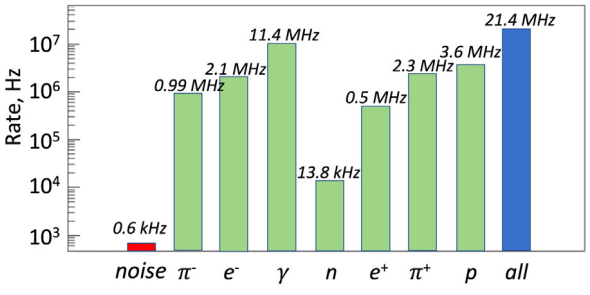

Fig. 70. Rates in the first SVT layer for a 5-cm-long liquid hydrogen target at the nominal CLAS12 operating luminosity of 10^{35} cm^{-2} s^{-1}.

Geant4-based calculations of fluences, radiation doses, and damage rates in the SVT were performed for different particles using the CLAS12 Monte Carlo simulation package GEMC [24]. The SVT rates were estimated for liquid-hydrogen, liquid-deuterium, carbon, iron, and lead targets. For each event, 124,000 electrons going through the target within a 248.5-ns time window were simulated. This corresponds to the full nominal CLAS12 10^{35} cm^{-2} s^{-1} luminosity on a 5-cm-long liquid-hydrogen target at 11 GeV beam energy. Rates in the first SVT layer for a 5-cm-long liquid-hydrogen target are shown in Fig. 70. For a carbon target at a threshold of 40 keV, the hadronic rate was estimated to be 5 MHz (total rate 40 MHz) with strip hit rates of 3.1 kHz (Region 1), 2.2 kHz (Region 2), and 1.7 kHz (Region 3). The energy deposited in layer 1 for the electromagnetic and the hadronic particles is shown in Fig. 71. At a threshold of 30 keV, 92% of the electromagnetic background is rejected while preserving 99.5% of the signals coming from the hadrons [31].

Simulations were performed to optimize the thickness of a tungsten shielding cylinder around the CLAS12 target scattering chamber inside the first SVT layer [32]. A 51-μm-thick tungsten shield was ultimately installed based on the results of these studies. The shield consists of 2 sheets mounted over the top and bottom halves of the foam cylinder referenced to the SVT common ground. The SVT rates and radiation damage benefit from the inclusion of the tungsten shield. The rates have been compared with beam data at several beam currents.

While the gamma fluences/doses show a dramatic decrease with the introduction of the shielding, the total fluences and doses decrease significantly for the thinner configuration and do not vary much for thicker tungsten (see Fig. 72). The photon radiation dose becomes negligible for 50 μm or more of tungsten with total 1 MeV equivalent radiation dose about 65 krad per year on a liquid-hydrogen target. For 15 years of running the experiment on a carbon target the estimated radiation dose for the sensors is 2.5 Mrad (with 50% operation) [31].

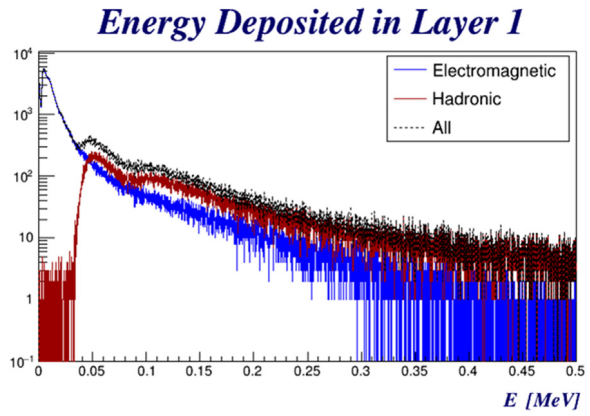

Fig. 71. Energy deposited in SVT layer 1 for electromagnetic and hadronic particles for a liquid-hydrogen target at the full nominal CLAS12 operating luminosity.

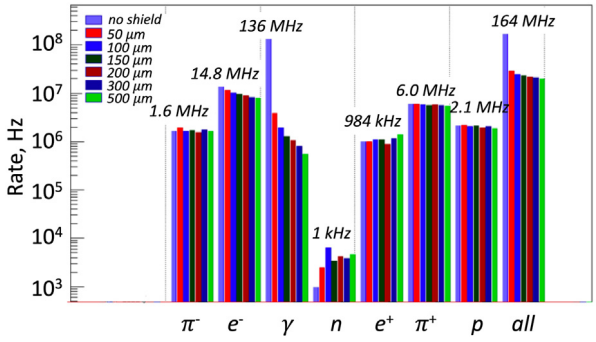

Fig. 72. Rates in the first SVT layer for different tungsten shield thickness from 50 to 500 μm for a liquid-hydrogen target at the full nominal CLAS12 operating luminosity. No energy threshold cut applied.

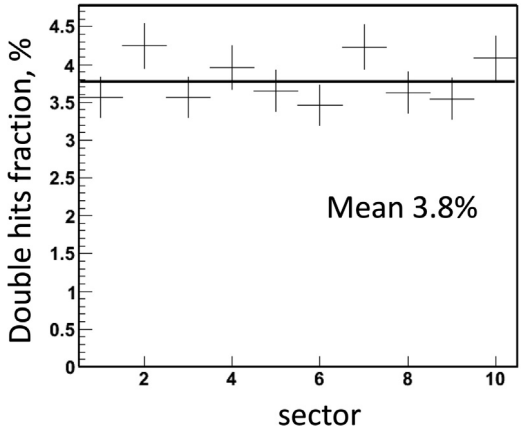

Fig. 73. Double hit fraction in SVT Region 1 with a 5-cm long liquid-hydrogen target at the full nominal CLAS12 operating luminosity.

An estimate of the double hit rate from background was performed. Double hits occur when a background hit and a track hit occur close enough in space to be reconstructed as a cross. Fig. 73 shows the double hit probability for the inner region of the SVT. The estimated fraction of events with double hits is 3.8%. The ratio of the double hits to the single hits was found to be about 1%.

8.3. Magnetic field

Due to the constraints on the maximum length of the cables, the readout, slow controls, and power supply crates are installed on a

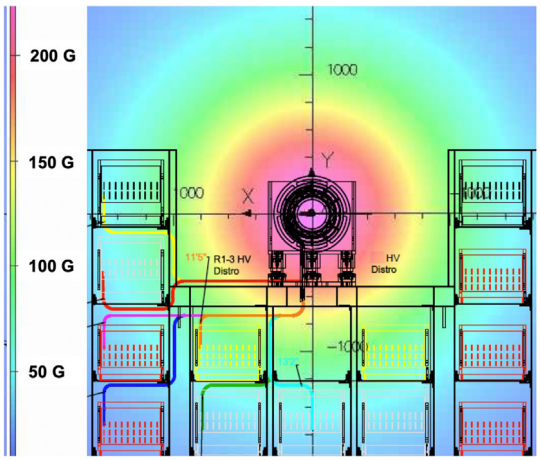

Fig. 74. Solenoid field map at the location of the SVT service cart.

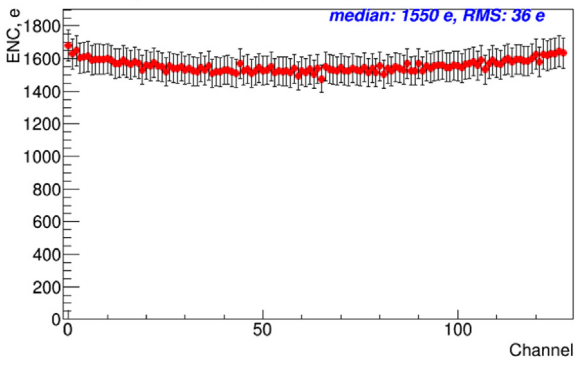

Fig. 75. Typical input noise on a single FSSR2 ASIC chip of an SVT module.

movable service cart within a few meters from the detector. To assess the potential impact of the solenoid field on the SVT data acquisition, a magnetic field map was simulated for the location of the power supply and readout crates. Fig. 74 shows that the maximum strength of the field at the crate location is at an acceptable level of 100 G.

9. Performance

9.1. Module testing

Detailed quality assurance procedures were developed for testing the modules during assembly at Fermilab, reception tests at JLab, tracker integration, and commissioning. At each stage the results were compared with previous measurements. The module performance was tested by the calibration procedures. No significant correlated noise has been observed between the channels of the same chip, chips of the same module, or closely placed modules. The measured average channel noise (see Fig. 75) is comparable with the estimated contributions of different noise sources. The gain dispersion measured on the channels is within the specifications of the readout chip (see Fig. 76). To verify operational stability and functionality of the module at low temperature with active cooling, a performance and burn-in test was conducted at −20 °C using a sealed container and a module in a carrier box, and the results were within the specifications.

Longer silicon strips have higher capacitance and thus a higher input noise (see Fig. 77). Noise calibration accounts for the different strip lengths and pitch adapter layouts that affect the input capacitance of the preamplifier. The mean noise values scale linearly with strip length, which confirms that the noise is dominated by the strip capacitance and not by coherent noise pickup of the system. The channel

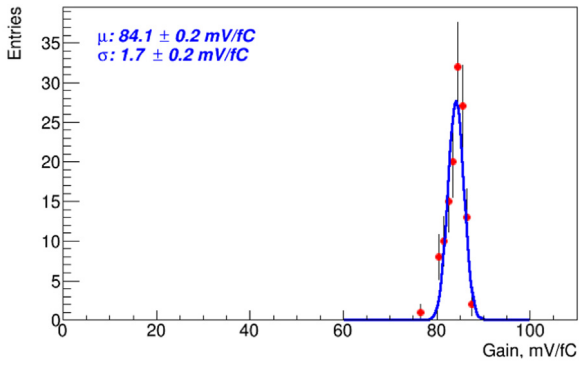

Fig. 76. Distribution of the gain for the channels of one representative FSSR2 ASIC.

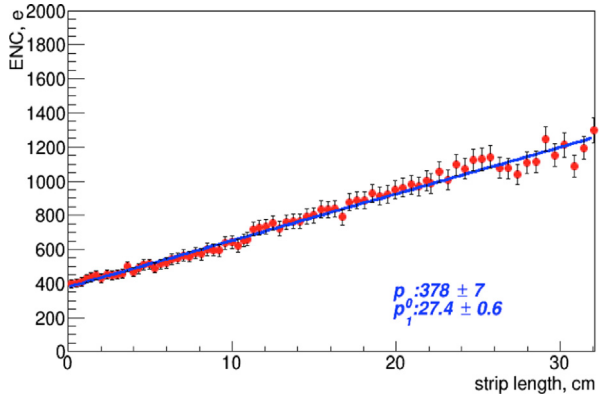

Fig. 77. Input noise vs. strip length of a typical FSSR2 ASIC. The results of a linear fit are shown.

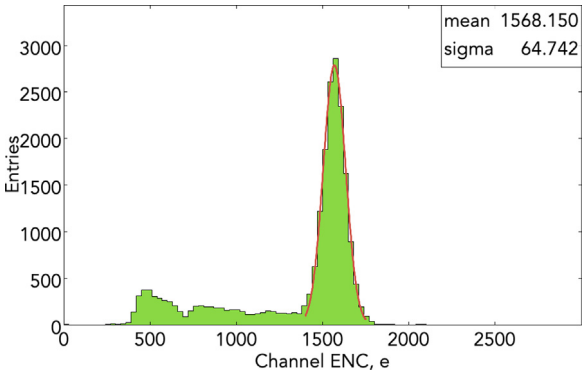

Fig. 78. SVT ENC for all channels. The main peak corresponds to the full length strips (33 cm). The shoulder on the left side is related to the shorter strips.

noise has a linear dependence on the strip length with an offset p_0 about 400 electrons (with shaper at 125 ns) corresponding to the ENC for the shortest strips and a slope p_1 of 27 electrons, consistent with FSSR2 noise measurements at comparable capacitive load taken on a single-chip test board with discrete capacitors (see Fig. 59).

The equivalent noise charge of the SVT channels is shown in Fig. 78. The peak is ~1600 electrons (signal-to-noise ratio 15), the shoulder on the left side is related to the shorter strips. The channel noise allows setting a 3σ threshold at the 30 keV level.

The detector response and full readout chain calibration was done with γ and β sources, cosmic muons, an electron beam, and a proton beam. The output from the 3-bit ADC does not allow for a good resolution of the pulse height. To increase the number of bins in the cluster charge distribution, a sliding window method was used,

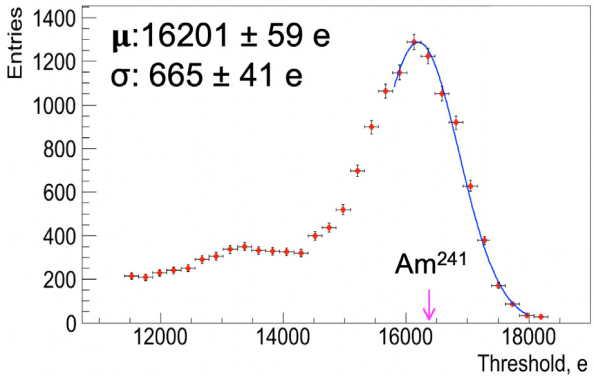

Fig. 79. Signal from Am^{241} γ source. The results of a Gaussian fit are shown and the expected peak position is marked with an arrow.

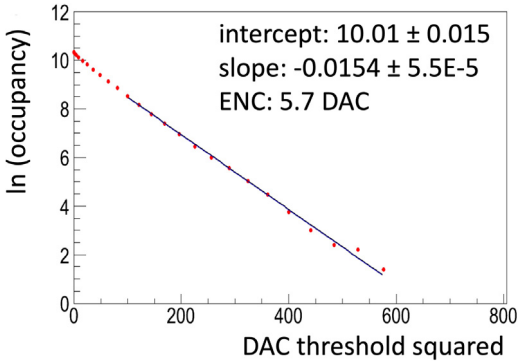

Fig. 80. Log occupancy vs. DAC hit/no-hit threshold (in DAC bins) squared. The results of a linear fit are shown.

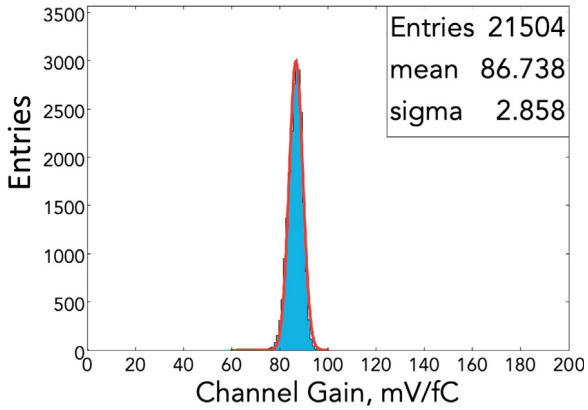

Fig. 81. Distribution of gain for the SVT channels. The results of a Gaussian fit are shown.

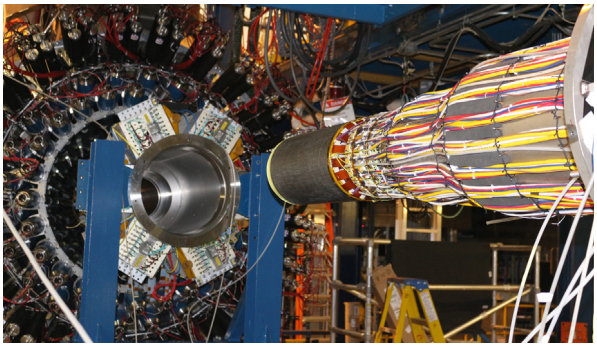

Fig. 82. SVT installed in Hall B before being integrated with the CLAS12 detector. The cables are routed through the slots in the support flange. The cooling pipes, insulated with foam, are attached to the bottom of the support tube.

combining the data taken for the same time window in several runs with discriminator thresholds set for the required binning. When using signals from minimum-ionizing particles, like cosmic rays or a ^{90}Sr β source, the signal distribution is fit with a Landau–Gauss convolution. The detector response to a MIP was about 24,000 electrons, which is what is expected for the 320-μm thick sensor. The results of absolute gain calibration with a γ source (Am^{241}) are shown in Fig. 79. The signal peak is in good agreement with the expected position (marked with an arrow).

9.2. Integration and system checkout

To verify the performance of the integrated detector, data acquisition chain, power services, and cooling system, as well as the detector control and data acquisition software, the final detector system was installed in the clean room and used at all stages of tracker integration and commissioning. The SVT was operated for several months under environmental conditions close to those in Hall B. Defects known before the integration of the system were reestablished. 99.9% of channels were operational after the detector integration.

The noise behavior was found to be within expectations and well understood. The dependence of the noise on the environmental temperature and humidity is small and the noise performance in Hall B was comparable with the results taken in the clean room during integration. Several diagnostic tools were used to measure the common-mode noise performance of the detector. The noise occupancy plot with no charge injection was used to find the noise value. This plot probes the tail of the noise distribution, which can show effects that are masked by the higher occupancy at low thresholds and provides a cross-check of the noise value obtained from the response curve measurement. A Most Probable Value (MPV) of the signal peak from a MIP corresponds to the 100th DAC bin. Fig. 80 shows the log occupancy vs. threshold squared plot. Purely Gaussian noise gives a straight line in the plot. Occupancy refers to the normalized total number of hits in all channels in a run. The power of this plot is to show non-Gaussian noise contributions as deviations from this linear fall-off. The hit map is plotted in the plane spanned by channel number and event number. It is an important diagnostic tool to test for the presence of the correlated noise and to understand the data quality, such as dead/noisy channels, channel occupancy, uniformity across the channels and events in a run, and coherent effects on the channels in individual events.

No significant correlated noise has been observed between the channels of the same chip, between the chips of the same module, or between the closely placed modules. The front-end electronics performed reliably, and no chip failures were observed. The distribution of gain was uniform and stable for all channels (see Fig. 81).

In the hall the SVT was dismounted from the integration cart, craned to the target level in the horizontal position using the mounting brackets on the support tube and a counter-weight system to balance the weight of the cables, which remained connected to the modules and coiled around the support tube during this operation. The support tube was attached to the Central Vertex Tracker service cart with the alignment system for final adjustment of the SVT along the beamline. The cart hosts the crates for the power supplies, back-end electronics, slow controls, and the dry air distribution system. The service cart can be moved along the beamline on rails, providing access to the detector during maintenance. The power, network, gas, and cooling lines are long enough to allow the cart to be moved up to 5 m upstream of the nominal SVT installation position. Fig. 82 shows the SVT detector after installation in Hall B. The SVT Faraday cage, insulated with foam, can be seen on the right side of the photograph. All modules were found

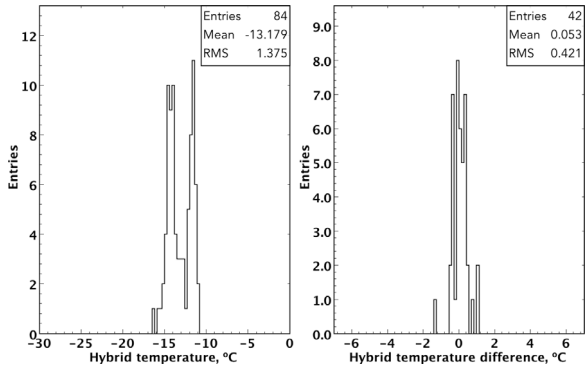

Fig. 83. Hybrid temperatures (left) and the difference in temperature between the two sides of the modules with the coolant at −26 °C (right).

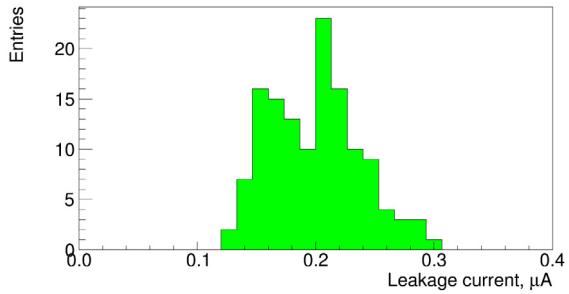

Fig. 84. Sensor leakage currents after detector integration. The spread in the distribution of the leakage currents is due to variations in the sensor temperatures.

to be fully functional after transportation from the assembly site and installation on the beamline.

The SVT barrel has no direct silicon temperature measurements. The spatially closest information available is from the temperature sensors on each side of the HFCB (between the FSSR2 chips) and from the ambient sensors on the upstream ring in the outer regions (see Fig. 47). The temperature variation of the SVT modules measured by sensors mounted on the hybrids with the coolant at −26 °C is shown in Fig. 83 (left). In these operating conditions the module temperatures were uniformly distributed within the region, with lower temperatures close to the cooling lines. The Region 3 temperatures were slightly higher than in the inner regions due to the design of the cold plate and longer lengths of the heat sinks (double-peak structure of the distribution). The temperature difference between the two sides of a module is within 1 °C as shown in Fig. 83 (right). The leakage current is extremely sensitive to temperature, doubling every ∼8 °C [33]. Sensor leakage currents remained at the same low levels after installation (see Fig. 84). The spread in the distribution of the leakage currents is due to variations in sensor temperatures. Thermal cycling of the modules verified the robustness of the bond wires.

9.3. Commissioning with cosmic rays

Cosmic ray tests of the SVT have been used to check track reconstruction routines for the SVT, to qualify the geometrical precision of the detector assembly by track-based alignment methods, to establish the correct readout, to verify good noise performance, to study the full response for the entire detector, to measure the inter-strip couplings, and to study the time evolution of the detector response. Once the reception tests of the first assembled modules were complete, a cosmic test stand was assembled (see Fig. 85) to verify the expected performance of the detector. Four SVT modules were stacked vertically between the two trigger plastic scintillator counters. Each scintillator

Fig. 85. The SVT cosmic test stand. Four SVT modules in their carrier boxes are mounted between the trigger paddles.

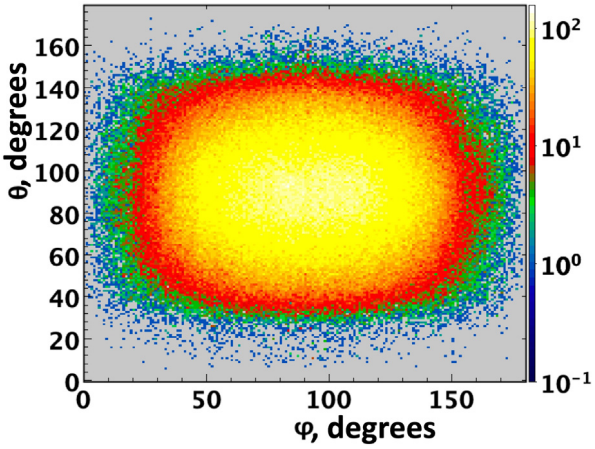

Fig. 86. Angular distribution of the cosmic muons reconstructed in the SVT.

was equipped with a photomultiplier tube (PMT) on one side. Evaluation of the signal-to-noise ratio and capacitive coupling confirmed the estimates and validated the full readout chain calibration data.

Cosmic data during detector integration in the clean room were taken in a stand-alone mode using the self-triggering feature of the FSSR2 readout chip in coincidence logic. VSCM boards reading the SVT modules located at the top and bottom halves of the horizontally placed barrel provided the trigger signals via the signal distribution of two VXS crates. The coincidence of signals from the trigger interface boards of both crates was taken as the cosmic trigger. With the logic described the trigger rate was ∼10 Hz. The response of the channels was uniform, and the performance results obtained during tracker integration were confirmed. The angular distribution of the cosmic muons reconstructed in the SVT is shown in Fig. 86, where θ is the polar angle and ϕ is the azimuthal angle. The tracks are uniformly distributed within the acceptance.

After installation of the SVT in Hall B and checkout of the detector services and readout system, a trigger from the Central Time-of-Flight (CTOF) detector [5] (located radially outward of the SVT) was used to collect cosmic data for the CLAS12 Central Detector. A cosmic muon reconstructed in the Central Detector is shown in Fig. 87. The SVT is the inner detector, surrounded by the Barrel Micromegas Tracker (BMT) [4], the CTOF, and the Central Neutron Detector (CND) [6]. The yellow circles represent crosses (matched hits on both sides of a module) in the SVT and the green circles correspond to the clusters in the BMT. Both tracking detectors have the same number of layers. The SVT has small angle stereo strips on the two sides of each module, and the BMT has interleaving layers of strips along the beam axis and arcs at fixed radii. Between the physics data taking runs more cosmic trigger data were collected for alignment, calibration, and performance

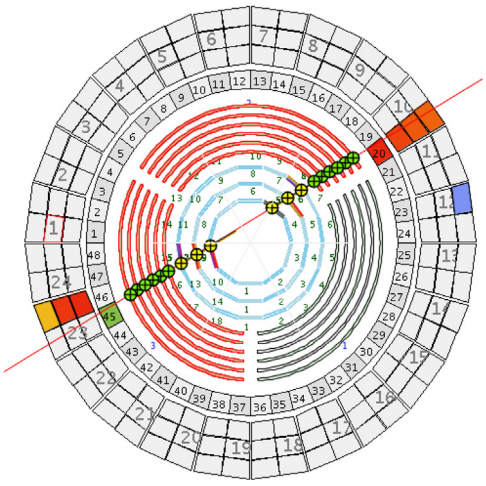

Fig. 87. Cosmic muon reconstructed in the CLAS12 Central Detector as seen in the CLAS12 Event Display (*ced*). The track is matched to the signal registered in the CTOF and the CND. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

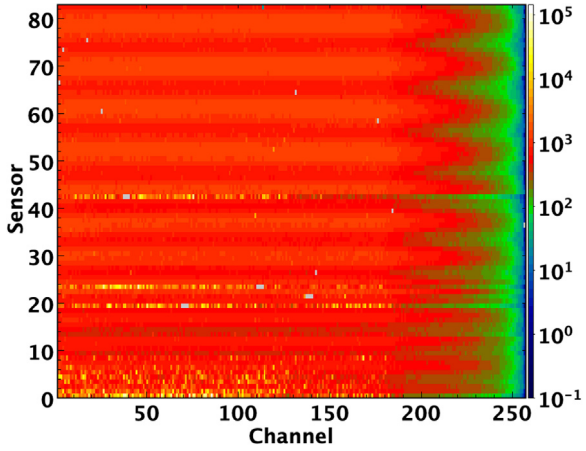

Fig. 88. Monitoring SVT hit map during a cosmic run showing sensor module vs. strip number (channel). The strips on the right side have shorter length.

studies. A hit map for the SVT channels during the cosmic run is shown in Fig. 88. Several sensors were under-depleted, visible on the plot as channels with higher occupancy. The lower hit occupancy on the right side of the map is due to the shorter strips.

The cluster size is affected by electronics cross-talk independent of the position where the charge was generated, and charge sharing among neighboring strips depending on the position where the charge was deposited. The charge sharing among two adjacent strips was studied using the η-function (also referred to as the response function), defined for the 2-strip clusters as the ratio of the pulse height of the left strip to the pulse height of the cluster, independently of which strip has the higher charge (seed strip). Fig. 89 shows the η-function obtained from the measurement of on-track clusters from cosmic muons. The distribution was obtained without applying cuts on the selected tracks. The granularity of the pulse height after the digitization is coarse due to the 3-bit ADC of the readout chip. The area where charge sharing occurs is large. There is a pronounced peak in the center between the two readout strips where all of the charge is collected by the intermediate strip. Because of capacitive coupling, signals on these intermediate strips are partially transferred to the readout strips.

The cluster size has been studied as a function of the local track angle. For normally incident tracks, the charge is shared at most between

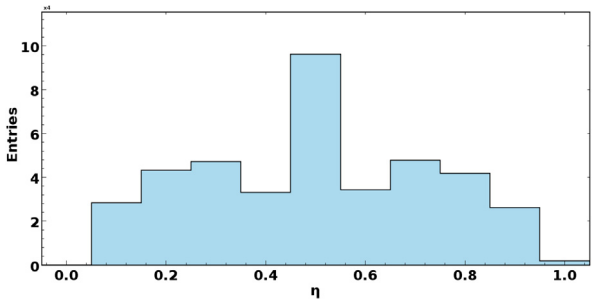

Fig. 89. Charge sharing in the SVT sensor: η-function for the two-strip clusters (see text for details).

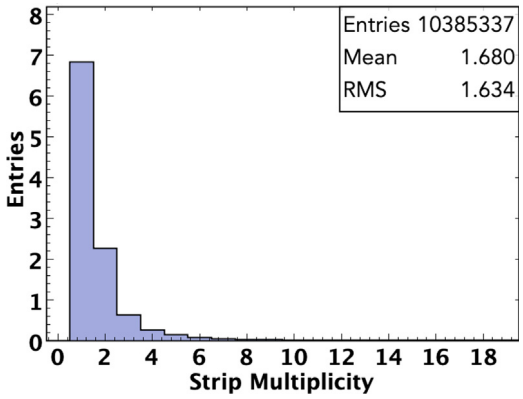

Fig. 90. Strip multiplicity of the clusters in a cosmic run. The mean cluster size is in agreement with the simulated data.

the two adjacent strips, although due to diffusion a small amount of charge may be collected by neighboring strips. The strip multiplicity of the clusters (cluster size) in a cosmic run is shown in Fig. 90. The size of the clusters is lowest in the innermost region and increases with radius due to a larger local track angle (the tracks, triggered by the CTOF, crossing the barrel far from the beamline). The few very wide clusters observed are attributed to muons with high energy, generating a shower in the detector. The results are in agreement with simulations and the data on the charge sharing among adjacent readout strips obtained during laser studies.

Cosmic muons are an important source for calibration and alignment. Their trajectories are sensitive to misalignments of the different tracker parts. The cosmic muons significantly improve the alignment precision. A preliminary alignment of the SVT was done using a sample of several million cosmic muon tracks taken without solenoid magnetic field. With exception of the modules located at shallow angles to the vertical axis, the acquired sample provided adequate statistics for the tracks to extract the misalignment data. The tracks crossing the sensors at large inclination angles and low-energy tracks subject to multiple scattering were rejected. An additional requirement on the χ^2 per degree of freedom of the track fit was applied to reject tracks affected by outlier hits. The spatial residuals before (blue) and after (red) the alignment procedure (see Fig. 91) are shown. Only the shifts in the sensor plane were taken into account in the alignment procedure for this plot. Validation of the alignment procedures was performed on Monte Carlo simulation and cosmic data.

9.4. Commissioning with beam

The performance of an SVT module was studied at Fermilab in a beam test with 120 GeV protons. The SVT module in the plastic carrier box was mounted vertically behind the CMS pixel beam telescope (8

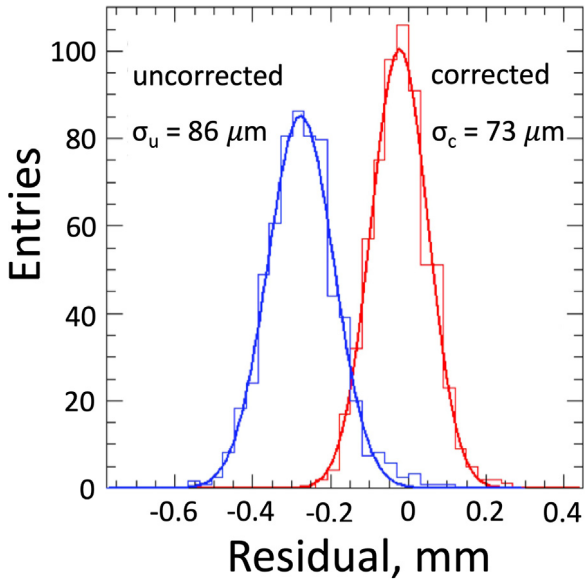

Fig. 91. Validation of alignment procedures on cosmic data. Residuals for one of the SVT sensors before (left peak) and after (right peak) alignment. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

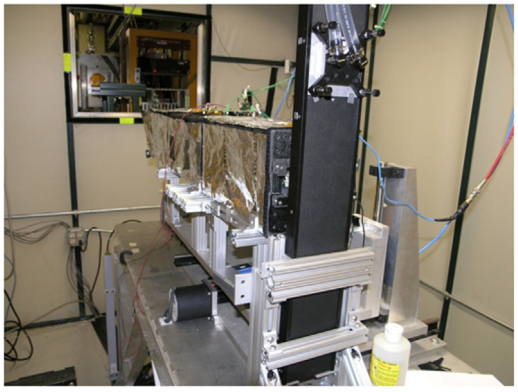

Fig. 92. Beam test setup at Fermilab. The SVT module in the plastic carrier box is mounted vertically downstream from the beam telescope. The hybrid side in on the top and the copper insert is attached to a water-cooled heatsink.

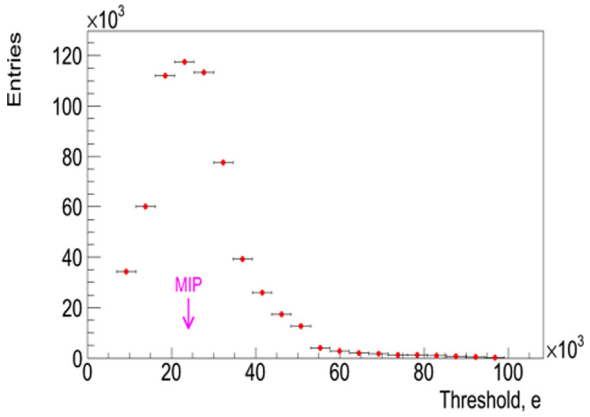

Fig. 93. Cluster charge distribution from 120 GeV protons. The expected MPV of the peak for a MIP is indicated by the arrow.

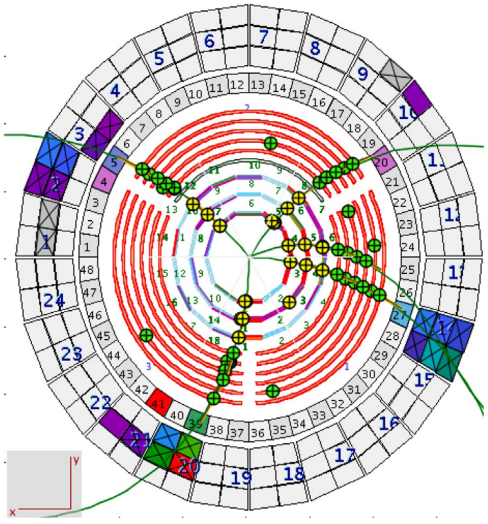

Fig. 94. Multi-track event reconstructed in the CLAS12 Central Detector during a beam run as seen in the CLAS12 Event Display (*ced*).

planes, ≈6 μm track position uncertainty, 2 cm × 2 cm active area), which was used as the trigger and the tracker. The beam test setup is shown in Fig. 92. The production SVT DAQ was exercised at different event rates. The event block mode was tested up to 100k protons per 4 s spill with no busy time. The signal-to-noise ratio was in agreement with the results with radioactive sources and cosmic muons. Several millions triggers were taken at different discriminator thresholds. The measured cluster charge distribution is shown in Fig. 93. The expected position resolution of the silicon sensors was confirmed.

The front-end electronics performance and noise occupancy of the detector were studied during physics data taking. No interference with other CLAS12 subsystems was found. The data quality and detector operational stability were verified with both online and offline monitoring packages. There were occasional FSSR2 chip latch-ups observed after the start of a new run. These latch-ups were traced to improper configuration settings of the chips and were fixed by adding additional resets to the run start sequence.

Tracks reconstructed in the CLAS12 Central Detector during a physics run are shown in Fig. 94. The level-1 trigger latency is finely tuned to match the CLAS12 trigger delays. Single Event Monitor (SEM) error checking implemented in the VSCM firmware allows real-time monitoring of the readout errors induced by the radiation. Relatively minor single event upsets were recorded in the SVT readout electronics with no latch-ups or single event burn-outs observed. The SEM recorded events are correlated with beam conditions in Hall B during the run. The SVT readout and power supply crates did not require rebooting. No readout or data corruption issues were observed [34].

The FSSR2 readout chip does not provide the timing information from the hit. Reading the time stamp associated with a hit was implemented in the VSCM board. The time stamp is synchronized with the "Got Hit" pulse from the chip when the pulse height reaches the threshold set for the first discriminator of the ADC. Timing of the SVT hits referenced to the CTOF timing are shown in Fig. 95. The data correspond to the time difference between the SVT and the CTOF time stamps for the SVT hits that were associated with a track. Applying a cut on this time difference can be used to remove background and noise hits in the track-seeding algorithm.

Radiation-induced energy levels in the middle of the band gap cause an increase in the number of thermally generated electron–hole pairs. Consequently the bulk sensor leakage current increases with the absorbed flux according to the empirical parameterization depending on the fluence, annealing time t, temperature during annealing T_A, and reference temperature T_{ref} as:

$$\Delta I_R = \alpha(t, T_{ref}, T_A)\Phi V, \tag{7}$$

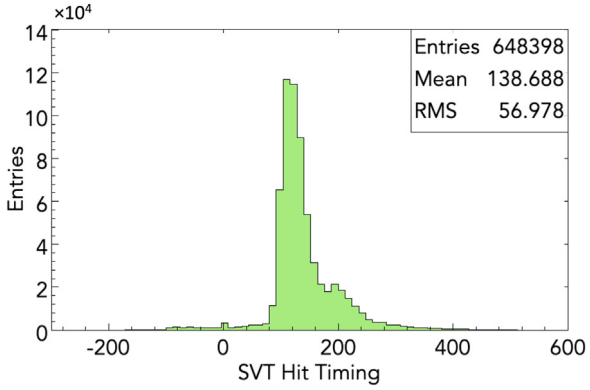

Fig. 95. SVT hit timing in ns referenced to the CTOF hit time in a physics run with the liquid-hydrogen target.

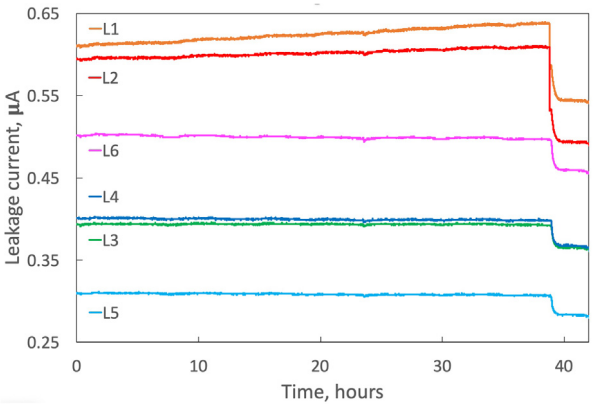

Fig. 96. Thermal runaway in the SVT inner layers (L1 and L2). The data shown correspond to the period right after the physics run, when the beam was turned off.

where Φ is the particle fluence, V is the volume of the sensor, and $\alpha \approx 4{\cdot}10^{-17}$ A/cm after 80 min annealing at 60 °C [35]. The raised leakage current increases the noise and heats up the sensor, which, in turn, will further increase the leakage current. When the temperature increases beyond a critical temperature where the cooling cannot maintain a stable temperature, this will result in thermal runaway. A feedback self-heating loop has to be counteracted with sufficient cooling. Fig. 96 shows thermal runaway in the two innermost layers of the SVT that received the highest radiation dose after beam operation. The leakage currents in other layers were stable. The monitoring data were taken after a physics run with a liquid-hydrogen target, when there was no beam in the hall for extended time. The leakage currents became stable when the coolant temperature was decreased.

Fig. 97 shows monitoring plots for the average sensor leakage currents in the SVT layers during data-taking with a liquid-deuterium target. For the first few hours in the time period shown there was no beam in the hall and the currents were stable. Currents in all layers increase with time when beam is present. The jumps in the leakage current of a layer between two values are related to beam trips. The largest difference between the beam-on and beam-off levels and the rate of current increase is in the inner layers. The distribution of leakage currents is in agreement with the accumulated dose, with higher currents in the sensors closest to the target. The sensors in the outermost layer have higher temperatures, affecting the currents. The data were taken at a 50 nA election beam current. For the unirradiated sensors, the lowest leakage currents were in Region 1, where heatsinks have the shortest length.

Comparison of the rates of leakage current increase with different targets is shown in Fig. 98. The rate of current increase with a

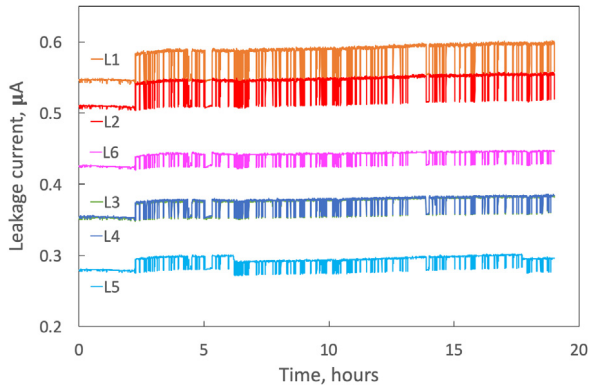

Fig. 97. Monitoring plots of the sensor leakage currents in the SVT layers during a run with a liquid-deuterium target.

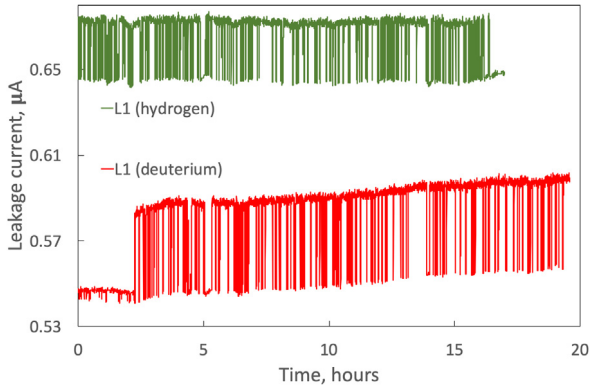

Fig. 98. Average sensor leakage currents in the SVT layer 1 during runs with liquid-hydrogen and liquid-deuterium targets. There was no beam for the first few hours for the liquid-deuterium target.

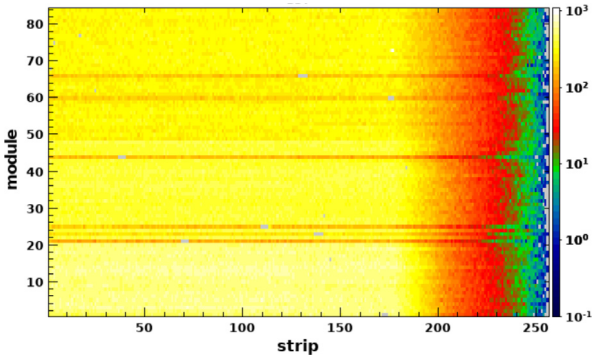

Fig. 99. SVT hit map during a physics run with the liquid-hydrogen target.

liquid-deuterium target was about 1 nA per hour. The rate for a liquid-hydrogen target was 0.06 nA per hour. The difference in rates can be attributed to the higher neutron flux in the CLAS12 Central Detector for the liquid-deuterium target. The increase of leakage current when beam is delivered to the target is also larger for the liquid-deuterium target. The data were taken at 50 nA beam current corresponding to the instantaneous luminosity of 0.7 $\times 10^{35}$ cm^{-2} s^{-1} per nucleon. The leakage current for the run with a liquid-hydrogen target is higher because it was taken after the run with a liquid-deuterium target.

The surface of the silicon sensors suffers from damage due to ionizing radiation. The damage affects the insulating properties of the SiO_2 layer between the strips and the aluminum electrodes that collect the charge generated by the photons and the charged particles. The

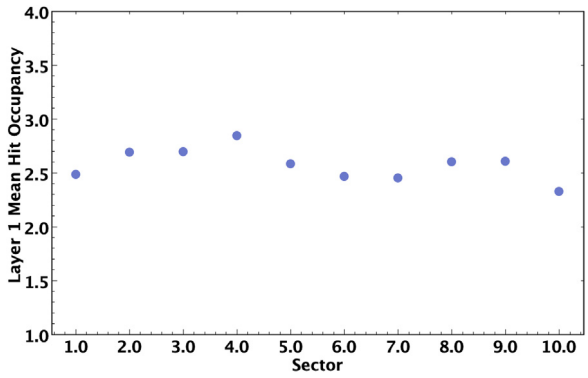

Fig. 100. Average number of hits for the sectors of the innermost SVT layer with a 5-cm long liquid-hydrogen target at 50 nA beam current.

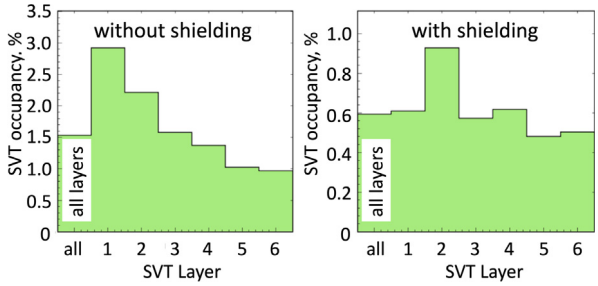

Fig. 101. Hit occupancies with and without the 51 μm-thick tungsten shield installed outside of the target scattering chamber.

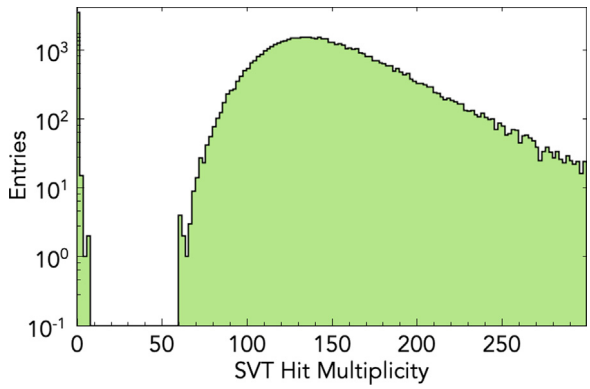

Fig. 102. SVT hit multiplicity during a liquid-hydrogen run at 50 nA beam current. The narrow peak on the left side represents the SVT occupancy with no beam.

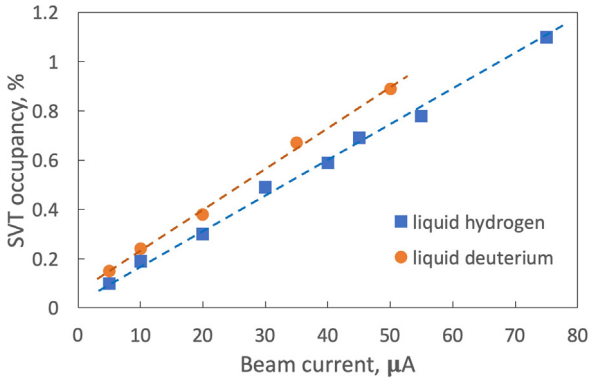

Fig. 103. SVT occupancy vs. beam current for the liquid-hydrogen and deuterium targets.

trapped positive charge causes an accumulation of electrons in the Si/SiO_2 interface between the strips, thus decreasing the resistance between the strips and increasing the interstrip capacitance, which affects noise performance and degrades the spatial resolution. After a year of running, several sensors developed pinholes (strips with DC current through the damaged dielectric between aluminum strip and implant, resulting in a high current flowing into a channel) observed as groups of adjacent hot channels. The performance of the charge amplifying chip is deteriorated by the high current flowing into a channel. The bias voltage on these sensors (high occupancy regions on the map) has been lowered to reduce the noise and the abnormally high strip leakage currents. High current going through the bias resistor could cause unsafe voltage on the input of the preamplifier if the coupling capacitor is damaged. The increased leakage current was reduced by decreasing the detector temperature. The sensors are kept below −10 °C to freeze the reverse annealing, interleaved with short periods at room temperature for the beneficial annealing. A hit map of the SVT from a beam run is shown in Fig. 99. Sensors with pinholes are seen on the map as darker horizontal lines due to reduced efficiency (underdepleted sensors) with strips of masked hot channels with no hits. In the absence of physics background the same sensors in Fig. 88 showed higher occupancy because the average hit multiplicity in the cosmic event is low.

Fig. 100 shows the average hit occupancy (number of hits) per event in the innermost SVT layer for the data taken with a liquid-hydrogen target at a beam current of 50 nA. The hits are uniformly distributed among the sectors with occupancies close to 1% (each sensor has 256 strips).

The impact of the tungsten shield on the SVT occupancy (see Section 8.2) is shown in Fig. 101. The occupancies in all SVT layers are substantially lower, which results in better tracking performance due to reduced combinatorics. The effect of the shield on momentum resolution is negligible [32]. For the liquid-hydrogen target the occupancy in the innermost layer of the SVT is approximately 1%, decreasing to 0.5% in the outermost layer. There is no hit efficiency loss due to the dead time of the readout system at such occupancies.

The noise performance of the SVT during physics data taking is demonstrated in Fig. 102, showing the SVT hit multiplicity during a liquid-hydrogen run at a 50 nA beam current. The main peak is at about 130 hits per event, which corresponds to 0.6% detector occupancy. The peak on the left side represents the SVT occupancy when there was no beam in the hall obtained with a random trigger. The plot confirms a good signal-to-noise ratio of the detector.

Fig. 103 shows the SVT occupancy vs. beam current for the liquid-hydrogen and deuterium targets. The production data were taken at 50 nA. The SVT occupancy increases linearly with luminosity and remains at low levels not causing a substantial drop in the track finding efficiency.

A series of dedicated Central Vertex Tracker alignment runs was done at low beam current without solenoid magnetic field. New alignment data are collected whenever the position of the Central Detector subsystems or the target has changed. The dependence of the residuals on the track parameters is explicitly taken into account. The alignment code uses the partial derivatives of the Distance Of Closest Approach (DOCA) taken with respect to the track parameters and the SVT geometry. This approach accounts for the correlated shifts among the geometry parameters. In addition to the track-based alignment, the data from the mechanical survey of the fiducials are also recorded whenever the detectors are moved. The centroid residual for one of the SVT sensors after preliminary tracker alignment is shown in Fig. 104. The sensor spatial resolution is within the specifications. Further improvements are expected from the ongoing development of the alignment algorithm and the track reconstruction code (like energy loss and

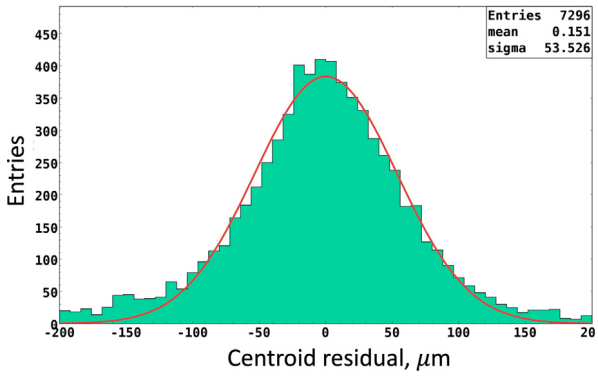

Fig. 104. Centroid residual for one of the SVT sensors after preliminary tracker alignment. The results of a Gaussian fit are shown.

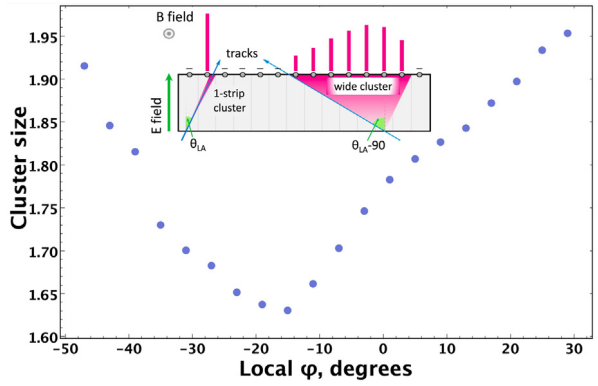

Fig. 105. Cluster size vs. local track azimuthal angle. The inset shows the dependence of the cluster size on the track angle. The smallest cluster size corresponds to the Lorentz angle.

Lorentz angle corrections that have strong impact on alignment). See Ref. [23] for more information.

In a strong magnetic field, charge in the silicon detector drifts at the Lorentz angle (the angle between the drift direction and the electric field), which must be taken into account when reconstructing the cluster position. Fig. 105 shows the average cluster size at different local azimuthal angles of the track. The zero angle is related to normally incident tracks. The data were taken at negative polarity of the solenoid field. The Lorentz angle θ_{LA} is independent of the track local angle and contributes to the charge spread among the strips. There is no compensation for the Lorentz angle in the orientation of the SVT sensors to minimize the cluster size for the tracks originating from the primary vertex. The Lorentz angle can be calculated as the track incidence angle corresponding to the minimum of the average cluster size when the track local angle is equal to the Lorentz angle.

The number of matched SVT hits per reconstructed track in the physics run with the liquid-hydrogen target is shown in Fig. 106. For most tracks all 6 SVT layers have been matched to a track. Tracks with a low number of matched hits passed through the gaps between the modules.

Fig. 107 shows the efficiency of matching the hits to the tracks in each SVT layer. For each layer the efficiency is the ratio of the number of tracks with hits in the layer associated with a track to the number of tracks with on-track hits in two adjacent layers. The lower efficiency in the outer SVT layer is due to the tracks that are not within its acceptance. The data were taken at 5 nA beam current with a 5-cm-long liquid-hydrogen target. The efficiencies are expected to improve with further development of the tracking and alignment algorithms.

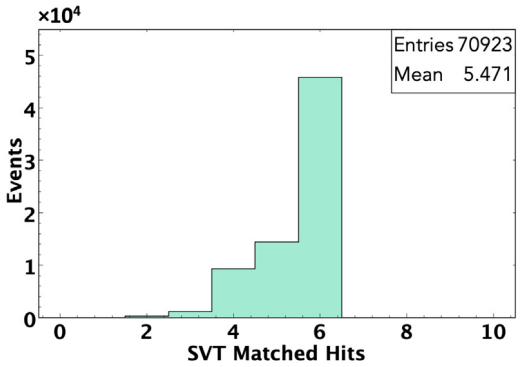

Fig. 106. Number of the SVT hits per track. For most tracks all 6 SVT layers have been matched.

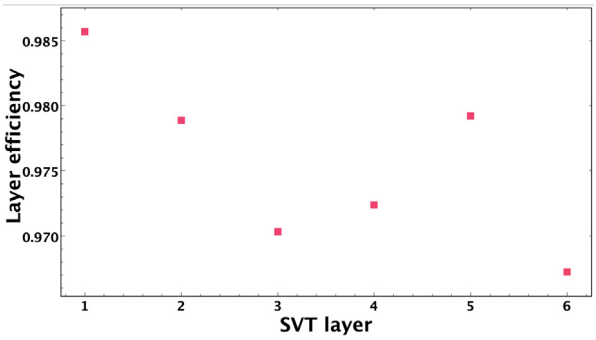

Fig. 107. Efficiency of hit matching in the SVT layers. The hit is matched if it is associated with a track and there are on-track hits in two adjacent layers.

Table 2
ENC of the silicon strip modules from the silicon strip trackers at CERN, Fermilab, and JLab.

Detector/ Module	Strip Length	ASIC	ENC
ATLAS barrel 6	12 cm	ABCD3A	1400 e
CMS TOB OB1	18 cm	APV25	1100 e
CLAS12 SVT	33 cm	FSSR2	1600 e
LHCb ST TT L	38 cm	BEETLE	3400 e

10. Conclusions

The SVT is installed in the CLAS12 spectrometer in Hall B of Jefferson Lab, and the performance of the modules measured during detector integration has been confirmed. No channels were lost during the installation. The SVT barrel has been electrically tested with the number of defective channels of 0.1%, well within the specification. The chip average ENC noise is uniform, ~1600 e, on par with the leading silicon strip trackers (see Table 2) [36–38]. There is no evidence of coherent noise between the modules and other components. The tracker has been commissioned with cosmic rays and integrated as part of the CLAS12 Central Detector. Experience in operating and commissioning the tracker has been gained during the first year of operation. The tracking performance was studied with beam data and matches the physics requirements.

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administrative and technical staff for their contribution to this project. We would like to thank the Hall B staff, the JLab Fast Electronics Group, the JLab Detector Support Group, and the Micromegas team for their generous support of the SVT project. We also thank the CLAS12 Collaboration for staffing shifts and taking high quality data. A special gratitude we give to Daniel Carman and Alexander Sukhanov for their comments and advice on this paper. This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Nuclear Physics under contract DE-AC05-06OR23177.

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